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Contributions to Converters in Single Phase Distributed Photovoltaic Systems

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By:

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This Thesis is Dedicated to

My parents, who sacrificed much for me and inspired me the meaning of success

My wife, who is the source of happiness in my life and my companion in the way of success

My children, who make my life full of beauty

Contributions to Converters in Single Phase Distributed Photovoltaic Systems

A Thesis Submitted to University of Plymouth in Partial Fulfilment of the Requirement to Obtain the Degree of DOCTOR OF PHILOSOPHY in Electrical Engineering

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Author's Declaration

At no time during author registration for a degree of Doctor of Philosophy has been registered for any other university award without prior agreement of the Graduate Subcommittee.

Work submitted for the research degree at the Plymouth University has not formed part of any other degree either at Plymouth University or at another establishment.

This study was financed by the Iraqi Ministry of Higher Education and Scientific Research.

A programme of advanced study was taken, which included the extensive reading of literature relevant to the research project and attendance of in class courses and international conferences on power electronics.

The author has published the work results in the following international conferences and a copy of the publication can be found in appendix A:

- The IEEE Transportation Electrification Conference and Expo Asia-Pacific 2016, Busan-Korea. The paper was granted Best Paper Award.
- The 17^{th} International Conference on Environment and Electrical Engineering (EEEIC 2017) Florence-Italy.
- PEDS 2015 the 11^{th} IEEE International Conference on Power Electronics and Drive Systems, Sydney-Australia.

Word counts in the main body of the thesis: 26700

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Abstract

This thesis contributes to improve the photovoltaic Distributed Generation (DG) systems by proposing three novel methods to the system. On DC conversion side, a new integrated magnetic structure for interleaved converter and a new method to calculate the eddy current and hysteresis losses in the magnetic core were proposed. On inversion side, A new synchronisation method for grid tie inverters was suggested. The technique is using the Recursive Discrete Fourier Transform (RDFT) to find fundamental in grid waveform.

On the DC converter side, the benefits of the new structure is to produce magnetic flux that alternate in the core across both directions of the B-H curve. The advantages of alternating magnetic flux are, to increase the Root Mean Square (RMS) value of produced current with respect to core volume that lead to reduce the core size and reducing losses by using high permeability material. Furthermore, the proposed structure led to reduce the number of magnetic components which helped to improve the efficiency. The converter was tested and evaluated were the results show that the topology is able to produce high gain and it shows that the new interleaved structure is efficient.

A new method to calculate the eddy current loss was proposed, where the flux waveform in the core was analysed to its original frequency component. Each of the components were utilized individually to find the loss. The effect of changing the duty cycle of the converter was taken into consideration on the total eddy current loss, as it will effect on the total harmonics content in the flux waveform.

On the inverter side, due to recent developments combined with the increasing power demand by single phase non-linear loads where voltage spikes, harmonics and DC component were impacted the electric grid quality. These effects can likewise make the synchronisation process a challenge, where filters or Digital Signal processing (DSP) analysers are required to acquire the fundamental component as a consequence to the waveform deformation.

A new linear approximation with RDFT is presented in this thesis for grid tie inverters. The new method provides a computation reduction as well as high accuracy in tracking the fundamental frequency in a distorted grid during synchronisation. The method accuracy was proved mathematically and simulated with different input signals. Error in magnitude and frequency measurement were measured, presented and compared with other research in order to verify the proposed method.

Contents

List of Abbreviations

ϕ: Flux.

B: Flux Density.

H: Flux Intensity.

μ : Permeability.

N: Number of turns

η: Turns ratio.

I: Current.

V: Voltage.

l: Length of a Magnetic field.

f: Frequency.

t: Time.

T: a waveform period.

P: Power.

P_t: total transformer power.

P_1: Power through primary windings.

P_2: Power through secondary windings.

V_{A1}: Voltage across A_1 windings.

V_{A2}: Voltage across A_2 windings.

F: Fringing factor.

ρ: Resistivity of a material.

A_c: Core cross section area.

l_g: air-gap length.

l_c: core length.

W_a: window area.

L: Inductance.

C: Capacitance.

R: Resistance.

r_i: internal resistance of an inductor

D: Diode.

ω: angular frequency.

α: Overlap duty cycle.

M: total number of the samples taken at a sampling frequency.

k: Fast fourier bin width.

G: magmatic core window length.

List of Figures

Glossary

AC Alternating Current. 16

DC Direct Current. 2, 12, 16, 44, 62, 80, 87, 114, 123

DCCM Discontinuous Current Conduction mode. 92

DFT Discrete Fourier Transform. 10, 11, 12, 14, 36, 41, 42, 43, 62, 63, 64, 65, 100, 101, 106, 110, 126

DG Distributed Generation. i, 1, 2, 3, 9, 15, 16, 44, 123

DSP Digital Signal processing. i, 3, 14, 66

EMF Electromotive Force. 24, 72

FFT Fast Fourier Transform. 107, 108, 109

LPF Low Pass Filter. 36

MMF Magneto-Motive Force. 21, 123

MOSFET Metal Oxide Semiconductor Field Effect Transistor. 2, 45, 48, 49, 91, 98

Op-Amp Operational Amplifier. 114

PLL Phase Locked Loop. 3, 32, 33, 62

PV Photovoltaic. 1, 16, 17

RDFT Recursive Discrete Fourier Transform. i, ii, 11, 12, 14, 63, 65, 101, 102, 103, 105, 106, 128

RMS Root Mean Square. i, 5, 9, 124

SMPS Switch Mode Power Supply. 3, 55

THD Total Harmonics Distortion. 126

VA Volt-Ampere. 1

Chapter 1

Introduction and Literature Survey

1.1 Background

Providing alternative sources to fossil fuel has become the goal for many scientists, due to increasing power demand and global warming phenomenon. The alternative renewable sources are varied such as hydro-generators, wind turbines and Photovoltaic (PV), the variation is led to have different requirement to make use of the renewable energy. Generated power capacity Volt-Ampere (VA) of the renewable sources can be varied, usually high VA sources are installed in a mode where the power flow can be controlled by dispatch centre, while for low VA rating the sources are usually installed at the customer side like on roof PV and low power wind generators. Unfortunately, the low power sources are designed to be connected to the grid directly without a power flow controller, this combination of source on load side is now known as DG.

Improving PV systems was the core of research for many researchers,

where some papers focus on the maximum power point tracing while other search for a better method of control or improving converters efficiency.

Because all of the photovoltaic energy sources are providing Direct Current (DC) with a variable voltage rating, which makes them not suitable to connect to the grid directly. Using inversion devices like solid state inverters combined with DC converter is a requirement to make the alternative sources usable, though there are still many limitations combined with using it. Those with solid state devices can cause power loss due to two things:

- Losses in the component as iron, copper losses and conduction losses in semiconductor.
- Losses due to the timing, such as during synchronisation, the inaccurate phase angle will lead to circulating current which causes loss.

Generally, increasing the number of parts or the size of magnetic components such as inductors and transformers will lead to increase the losses. The phase angle and the switching time of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) can likewise contribute in increasing the losses.

In photovoltaic DG systems, while the energy transfers to the load, it must be processed to comply the load standard. The process is performed by a multi-stage system with different types of converters, such as DC-DC converter and inverter. This research will focus on improving the performance of converters in different sections of photovoltaic DG.

1.2 Motivation

This research is motivated to contribute in improving photovoltaic DG, Where in such system, there are many factors that can effect the performance as it

will be discussed later in this research.

Because photovoltaic DG systems were under development in many areas, investigation to contribute can be a challenge. This thesis focuses on two areas which are the DC converter and the AC inverter.

Voltage boosting using the conventional boost converter with high power capability can cause efficiency problem, where large duty cycle should be used and that will leave an impact on losses and power capability. Many research discusses how to improve the performance by presented a circuit modification such as by adding gain multiplier or increases the number of phases. This research will take the modification a step further by proposing an integration of the converter magnetic structure that can improve efficiency.

During the test of improved integrated structure, a difference between the actual iron losses and the calculated ones found. That difference motivated the researcher to investigate the loss mechanism, which lead to found a new method to calculate the eddy current and the hysteresis losses.

On the inverter side, distortion of the grid waveform due to low power factor electronic loads or non-linear load was the reason to investigate to find an accurate method for inverter synchronisation. Furthermore, taking into consideration the futuristic developments, synchronisation can be a challenging due to noise, where the carrier frequency of the inverters and transient effect of switching sources On and Off can effects on the zero crossing detector and Phase Locked Loop (PLL) methods.

The study leads to proposing a novel algorithm of synchronisation for grid tie inverters. The new method employs the use of DSP and high speed micro-controller. The algorithm may not be the optimum method of synchronisation as it contains calculation error, this will be discussed later.

1.3 Literature Survey

1.3.1 On DC Power Conversion

Boost Converter This type of converters was the initial type of voltage boosting Switch Mode Power Supply (SMPS). It consists of chopper such as a transistor, rectifier diode and a capacitor filter. The gain of this converter will mainly controlled by controlling the duty cycle of the chopper. An early research [1] presented the boost converter as a power factor correction device. The research studied frequency response of the converter and it results shows that the gain of the topology was subject to frequency changing [2]. Later, boost converter was implemented as a bidirectional in DG by [3]. The research concludes that the bidirectional boost converter has a superior efficiency in comparison to other converters.

Tapped boost converter was first presented and analysed by [4], as shown in figure 1.1. It can be considered as one of the solutions to increase boost converter gain. This topology was improved by having different number of turns between the output and tap point to obtain multi-output [5]. The tapped inductor topology is still facing a problem of low efficiency as [6] provides that the efficiency can be reduced significantly with the incrementing of output power.

The duality principle of using two converters was investigated by [7]. The research shows the use of half bridge with boost topology to construct DC converter that can act as a current source.

The idea of duality principle is used in this research by combining tapped inductor and interleaved boost converter topologies as it will

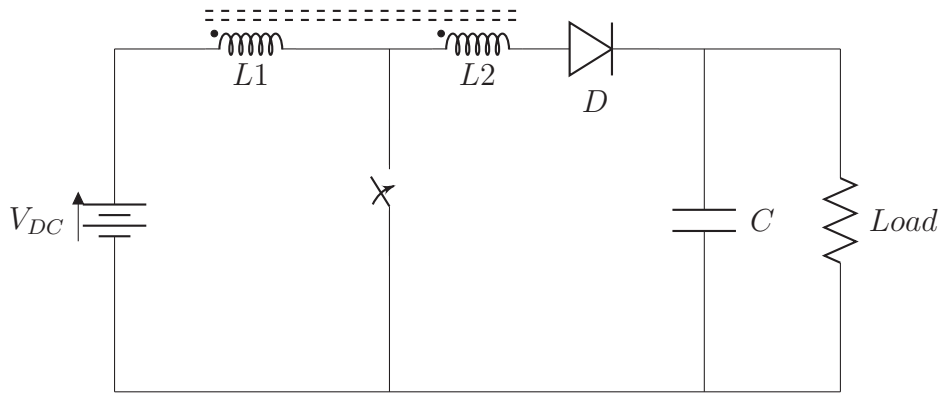


Figure 1.1: Tapped inductor

be showing later.

High Current Handling Capability interleave type of boost converter can handle, due to the multi-branches that the topology has as it was used in different applications [8, 9].

Integration [10] was the first to propose a magnetic component integration for interleaved buck converter, the work analysed the techniques of integration and found that coupling the converter inductors to alternate flux, can reduce the structure size as shown in figure 1.2. The research proved that the RMS values were highest in alternate coupling technique which can indicate a very efficient coupling. However, it can lead to an increment in the copper losses due to high RMS values.

[11] expanded the number of interleaved converter phases to three by using one integrated magnetic, likewise presented an analytical method to find the input current ripple based on the magnetic material reluctance and operating frequency. The research demonstrates that the topology has high power handling capability

Efficiency : Improving DC converter efficiency is one of the research con-

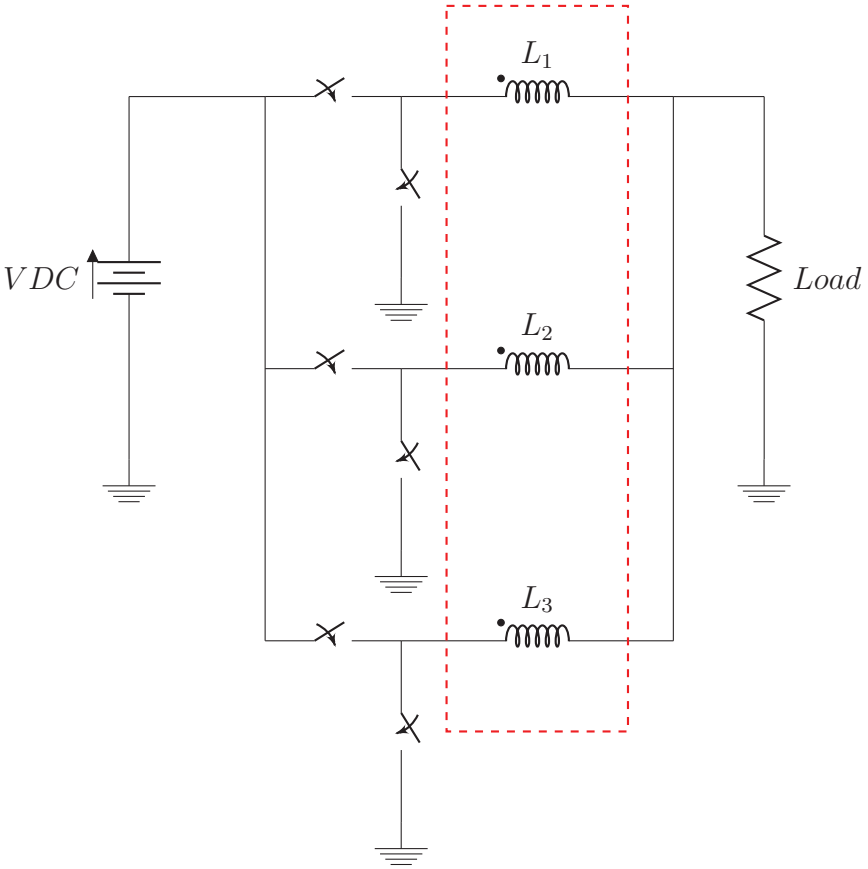


Figure 1.2: Inductors Integration

cerns. One of the factors that is limiting the converter's efficiency is the number of magnetics that are used per unit gain [12], where obtaining high gain requires using multi stage converters which need magnetic cores in each stage. [12] proposed in his work to combine all the boost converter inductors and the isolation transformer on one magnetic core.

[13] improved the design by reducing the flux density in the core which can improve the power capability and reduce the losses, where flux density reduction can reduce the iron losses in the core.

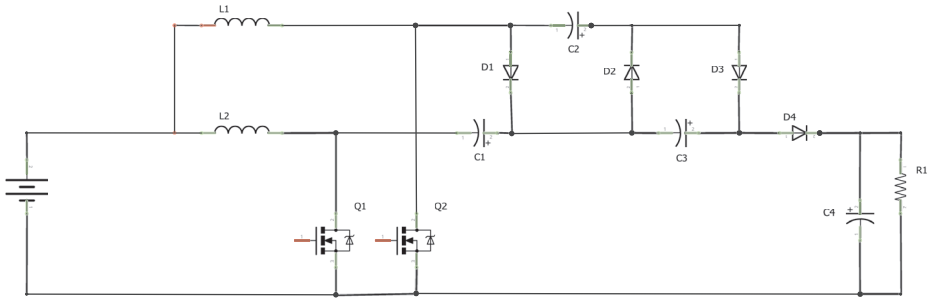
Minimizing residual flux : Another component integration was proposed

by [14], where two interleaved converters shared the same magnetic core as shown in figure 1.2 to construct the input inductor. Furthermore, they considered introducing an overlap time for the interleaved converters which will lead to an increase in the operating frequency and reduction of the core size [14].

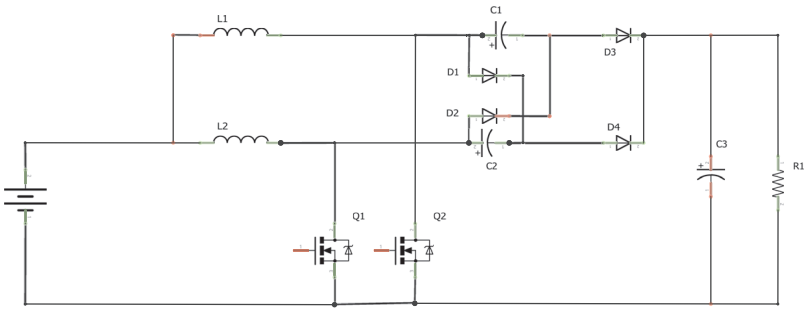
The integration of combining the inductors and transformer in DC-DC converters improved the efficiency, power handling capability and reduced the cost [15] in the interleaved boost converter.

Gain of Interleaved Boost : Because the use of this converter is to obtain high gain without compromising the efficiency, in recent years researches made an improvement in the transfer function by tweaking the converter circuit. The modification was done by adding a voltage multiplier that can improve voltage gain as in [16–19] as shown in figure 1.3a. The multiplier circuit in the research shown in figure 1.3b uses two extra diodes and two capacitors, the circuit will act as a voltage doubler to increase the gain and it contributed to improve system efficiency to 97%.

Transformer was likewise used as a voltage multiplier , it was firstly presented by [20], others preferred using coupled inductor to improve boosting as with [21, 22].



(a) Luozhou Suggested circuit



(b) Zhang Suggested circuit

Figure 1.3: Interleaved Boost Converter with Multiplier

Increasing the Number of Phases of the interleaved boost converter. Many researchers suggested to improve converter gain by increasing the storage elements number and this can be achieved by increasing the phases [23]. Though such configuration will require more switching elements and as consequent this will cause more losses.

Losses calculation : Classically [24], the losses were calculated by assuming that the magnetics were supplied by a sinusoidal current waveform. In 1988 [25] provided a theoretical and experimental results for the eddy current losses under square wave excitation, the results show that the loss is smaller in square wave excitation in comparison to sinusoidal waveform. [26] proposed an improvement to calculate the losses in magnetic laminations though the research did not cover the excitation under square wave. then [27] provides a study on the magnetic losses under biased and asymmetric excitation waveforms and compares them to sinusoidal excitation. However, the study did not cover how the asymmetrical waveform affects the losses. In 2013 a research [28] studied the effect of harmonics on transformer losses. The analysis of the research shows that the losses were increased if the flux waveform is distorted by harmonics.

1.3.2 On Synchronisation

Because most of DG's are uncontrolled by the dispatching centres, the micro-inverters in DG should have the ability to perform an accurate on-line monitoring to grid situation.

The monitoring process can be challenging due to grid diversity. Where different type of loads and power sources are connected in parallel,

which can lead to cause a distortion in the grid waveform and impact the synchronisation process. ie. Increasing single phase electronic loads with low power factor can increase the third harmonic at the load side or generate asymmetry in the waveform, likewise sudden load change or transient can cause signal fluctuation. Finding the true RMS value of pure sine wave can be easily done, while it can be long process when the waveform is distorted as it will require filtration or advance synchronisation technique. Previous research have investigated synchronisation to the grid under abnormal condition of operation such as [66]. The researcher was able to combine the effect of transient event in the grid and adding a DC component to the waveform to represent it.

There are many techniques that can be used to perform phasor synchronisation, such as using a phase locked loop (PLL) [29], Zero Crossing Detector, Discrete Fourier Transform (DFT) in digital systems and modified zero crossing detector [30]. Generally, digital PLL's and zero crossing detector are low in reliability when there is a DC component in the grid waveform such as transient and that due to device saturation and losing lock [31]. Where both PLL's and zero crossing detector relying on measuring the peaks of a waveform and assume the mid point is the crossing point. This assumption is not true when the fundamental if a signal contain harmonics or asymmetry is presented. Therefore, DFT is becoming more widely used in analysis of fundamental component and harmonics of electric utility voltage and current.

Sliding Window DFT research presented by [32] were the first to utilize real time DFT in power system. The research measures the angle of positive sequence voltage phasor to track the rate of change in network frequency. Recursive phasor computation shown in figure 1.4 was pro-

posed and the input test signal was filtered by the presented algorithm.

[33] presented two techniques, one was relying on the DFT window width by matching it to the period of the signal, while the second was relying on calculating the phase offset by comparing it to known phase.

Calculating the effective admittance in frequency domain and estimating the frequency was presented in [68], while [69] estimate admittance by decomposition the current waveform using RDFT.

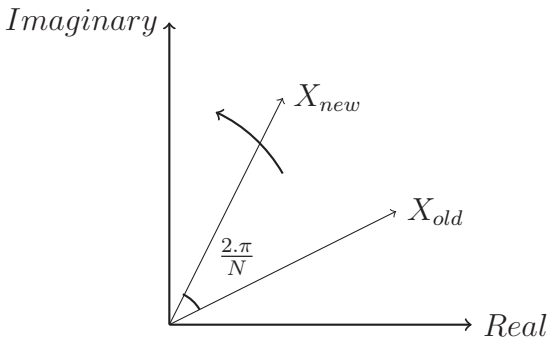


Figure 1.4: Inductors Integration

Where this algorithm rely on creating a Fourier BIN that has a width that matches the wavelength of the waveform as it will be explained later. This should filter any other unwanted harmonics and allow accurate measuring.

Compensating Phase Shift [33] and [34] suggested an improvement on using the DFT for synchronisation by compensating the phase shift when the time window does not match system period. the compensation uses two methods, the first to adjust the window by changing the sampling rate, while the second will calculate the phase error.

In research [67], the researcher focused on the estimation of phase angle

based on calculating the phase error of positive sequence of three phase system.

1.4 Outline of Thesis

With the increasing of using renewable energy sources, finding an effective method to boost the DC voltage has become a need.

The work is divided into five chapters: chapter one, contains the introduction and previous research work. The steps of how the integrated structure boost converter been developed and how it managed to increase the handling power capability without compromising the efficiency. It as well covers the aim and it will demonstrate the contribution to knowledge.

Chapter two covers the theoretical background and the principle of operation of different types of voltage boosting converters, losses associated with the magnetics and its calculations. Likewise the design proceeder of high frequency transformers is covered. On the inverter side, the chapter demonstrates the theoretical background of required tools for synchronisation such as DFT and RDFT .

Chapter three, introduces the new integrated structure of the interleaved boost converter and discusses the improvement of voltage gain. A new method to calculate the eddy current loss in the integrated structure was proposed and a mathematical derivation was explained.

A prototype was built and test results of the DC converter operation and behaviour are shown. A comparison was made to illustrate the difference and the effect of calculating the iron losses in magnetics using the new proposed method against the traditional method is discussed.

Chapter Four, demonstrate the use of straight linear approximation with RDFT for grid synchronisation was discussed. A software to execute the proposed algorithm was written and interfacing circuit was built to connect the ST discovery board. The algorithm accuracy was tested and results were analysed.

Chapter five contains the future work to improve the proposed methods and it will contain the final conclusion of the thesis.

1.5 Contribution to Knowledge

The main contribution of the thesis can be characterized into three parts as follows:

A New Method to Analyse Eddy Current Loss in an Integrated Magnetic structure for Boost Converter

A new integrated structure for the interleaved boost converter was proposed and implemented. The structure includes two main windings and two multipliers on the same core. The method suggested to wind the transformer is to alternate the flux in the structure. A new method to calculate the eddy current loss of the used core is presented. The method takes into consideration the effect of harmonics content at different duty cycles on the eddy current and hysteresis losses in the core. A prototype was built and test carried out to verify the performance and the analysing method.

An Adaptable Interleaved DC-DC Boost Converter

A new topology for an interleaved boost converter is presented. The circuit was able to provide high voltage gain without the need for using the large duty cycle as shown in the transfer function. Analysis showing the effect of input inductor winding loss in relation to the duty cycle. Losses

in semiconductor components are considered and analysed. Experimental results for a 200W prototype to boost 32V to 320V are presented and verified the design.

A New Method for Grid-Tie Inverters Synchronisation Based on RDFT with Linear Approximation

A new method based on linear approximation of RDFT is presented which will provide a computation reduction as well as high accuracy in tracking the fundamental in the distorted grid during synchronisation. Due to recent developments combined with the increasing of power demand by single phase non-linear loads, voltage spikes, harmonics and DC component had affected on the electric grid quality. These effects make Synchronisation a challenge where filters or DSP analysers are required to acquire the fundamental component as a consequence to the waveform deformation.

Applying DFT using DSP processors can be one of the best solutions to find the waveform parameters. However, the DFT is combined with high mathematical computations and required using advanced microprocessors to be applied in real-time.

Chapter 2

Theoretical Background

2.1 Key Definitions

2.1.1 Distribution Generation DG

DG typically means generating power in small scale at the end point of distribution system [35]. In late 1998 the term DG has become more common due to the increasing in the number of sustainable sources in US [36]. By relying on the modern technology in using renewable energy sources [37] and with the global trend to reduce the carbon emission , the traditional power system sections had changed and new terms have been used in the description. Energy sources in the DG can be either rotating machinery, such as wind turbines or synchronous machines, or static sources, such as solar and fuel cells [38].

Normally the total generated power by the DG is uncontrolled by flow controller but there is a bidirectional switch installed to isolate the source.

Figure 2.1 shows a radial single line diagram for the power system network with star connected laterals, where the DG is highlighted by dotted square.

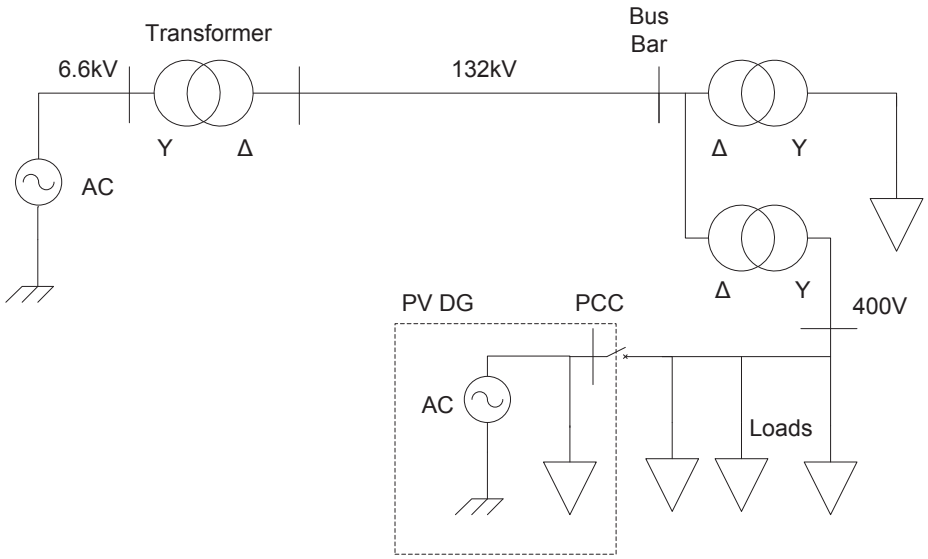


Figure 2.1: Single Line Diagram Shows The DG in the distribution system

There are different topologies to connect the PV to the source, where some are providing ground isolation at the DC converter side while others are isolating the ground using transformer at the Alternating Current (AC) side. Figure 2.2 demonstrates the system blocks diagram of the photovoltaic DG [39], where the ground isolation is at the inverter side .

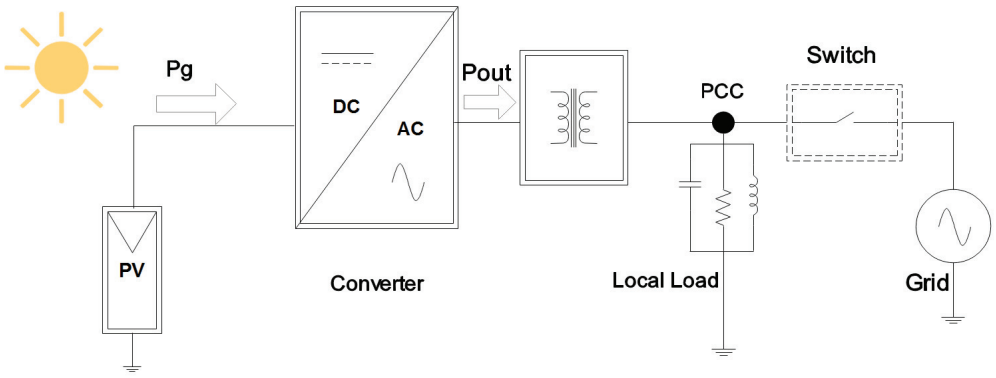


Figure 2.2: Power Flow Diagram of Distributed Generation

There are many advantages in implementing PV-DG for the consumer such as [40]

- Improve system reliability, where increase the number of sources will reduce the probability of power cut during generation fault.
- Improve power quality
- Reducing the power demand on the load side will contribute to increase network efficiency by reducing losses in the transmission and distribution.
- Reduce cost.
- Contribute in reducing pollution.

likewise there are advantages for the system as a stand alone such as

- Reduces losses in the transmission and distribution by reducing power demand.
- Increase system capacity
- Increases the control over the reactive power
- Provides environmentally friendly power

2.1.2 Photovoltaic Panel

PV panel is constructed of a set of solar silicon crystalline cells that are connected in serial/parallel groups in one frame. The silicon crystalline is forming a p-n junction, illumination the junction will generate charge pairs whenever light is absorbed. This action is similar to the photosynthesis and

will lead to pull the minority through the junction causing electrons flow [41]. The equivalent circuit of a PV cell is shown in figure 2.3.

The I-V characteristic of the PV is smiler to a single p-n junction characteristic as shown in figure 2.4, which can not make it considered as voltage or current source. The cell acts as a voltage source between the open circuit voltage to the maximum power point, wihile it acts as a current source between maximum power point to short circuit as in 2.4. This specific feature requires power management device to make the generated electrons flow useful.

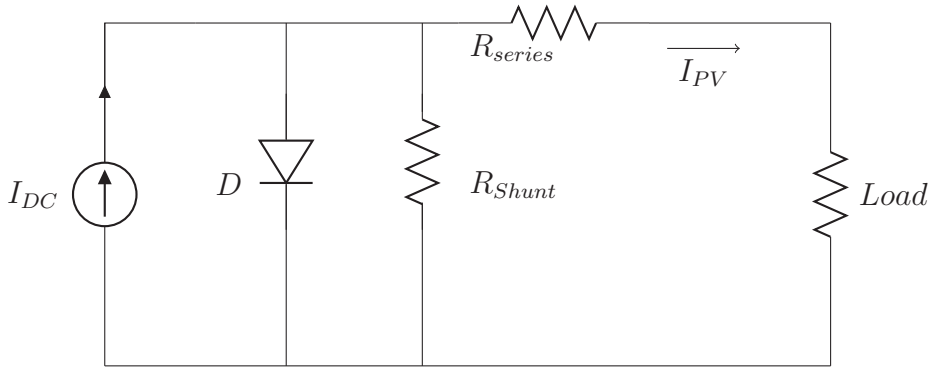


Figure 2.3: The Equivalent Circuit of Photovoltaic Cell

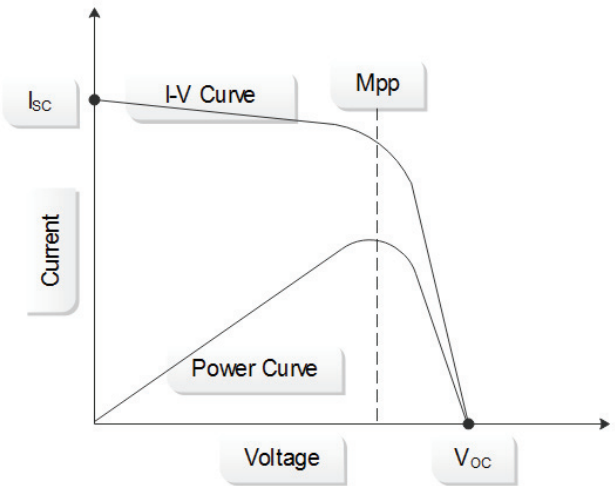


Figure 2.4: The IV Characteristic of Photovoltaic Cell

2.1.3 Flux Density B

Can be defined as the value of flux that has existed in the unit area.

$$B\ (Tesla) = \frac{\phi\ (weber)}{Area\ (m^2)}$$

The value of flux density depends on the media type, usually it is limited between zero to B_{sat} which is the saturation value.

B_{sat} is the maximum value of flux that can exist through a unit area. likewise It can be described as, the increment of magnetic field intensity H will not produce more flux to be exist through a unit area of the material as shown in figure 2.5.

However, even when the material is saturated there will be a small insignificant incrementing in the flux density. This increment is due to the absolute permeability of the air $\mu_o = 4\pi \times 10^{-7}$.

Saturation occurs because all the domains in unit volume of a material responded to external force (magnetic field). B_{sat} can differs depending on

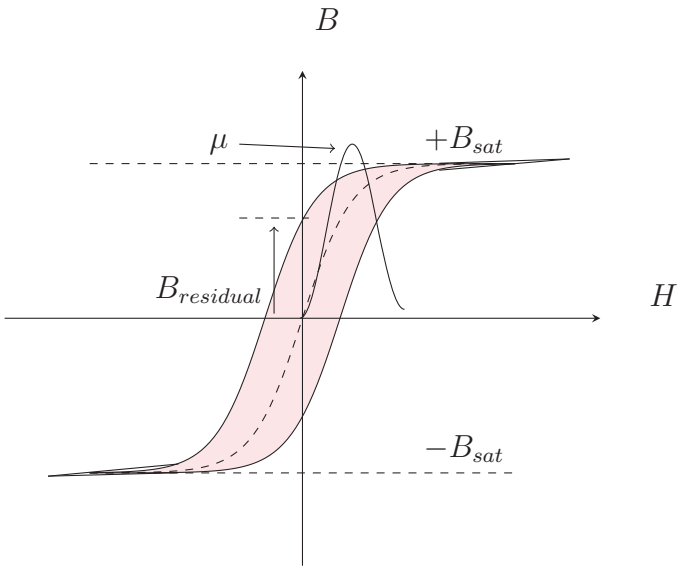


Figure 2.5: Hysteresis Loop

material substances as shown in the table 2.1 [42]. The value of B_{sat} can likewise be affected by temperature variation. Where, during operation the core temperature will rises which lead to reduce the flux density required to reach saturation, thus care must be taken to choose the operating point which can help to prevent saturation during operation, as shown in figure 2.6 [43] .

Material	Flux Density B_{sat} (Tesla)
CoFe (49% Co, 49% Fe 2 V)	2.2
SiFe (3.25% Si)	1.8
NiFe (50% Ni, 50% Fe)	1.5
NiFe (79% Ni, 4% Mo, Balance Fe)	0.75
NiFe Powder (81 % Ni, 2% Mo, Balance Fe)	0.8
Fe Powder	0.89
Ferrites Such as MnZn	0.4-0.5
Amorphous Metal Alloy (Iron-Based)	1.5

Table 2.1: Saturation of Various Magnetic Materials

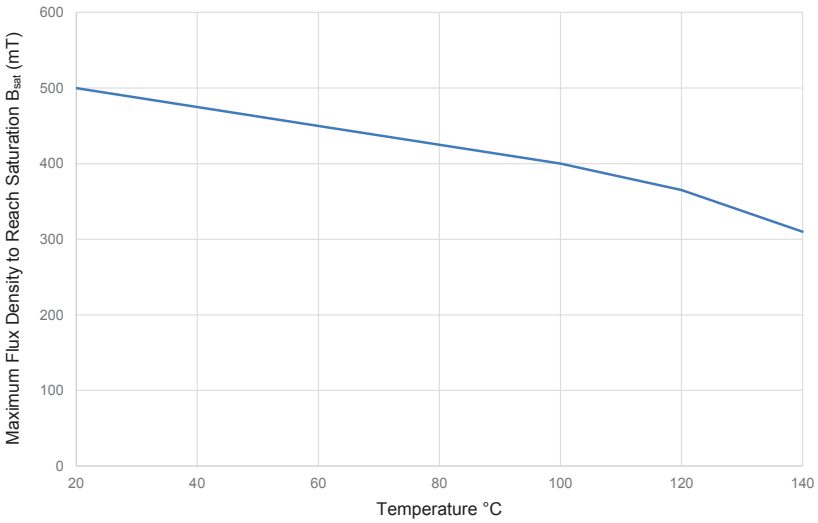


Figure 2.6: Flux Density Required to Reach Saturation B_{sat} in mT versus Temperature for MnZn

2.1.4 Magnetic Field Intensity

When an electrical current I passing through a conductor that forms a coil has N number of turns around magnetic core, a magnetic force Magneto-Motive Force (MMF) will be created. If we applied Ampere's law to a closed loop around the core that has a length of l [44], then

$$H = \frac{N \cdot I}{l}$$

where H is the magnetic field intensity $Amp \cdot turn/m$

2.1.5 Permeability μ

Is the relation between the establish magnetic flux density B at each point of the magnetic field intensity H it measured by $henries/meter$. Magnetic materials can be classified based on their permeability value. Where the ferromagnetic materials have high permeability value [45].

$$\mu = \frac{B}{H}$$

The permeability has a non-linear characteristic as shown in figure 2.5, while the curve will form a flat line during saturation. Temperature has its impact on the permeability value, as shown in figure 2.7, where it can leave an effect on the designed coil inductance during operation as the core temperature rises [46].

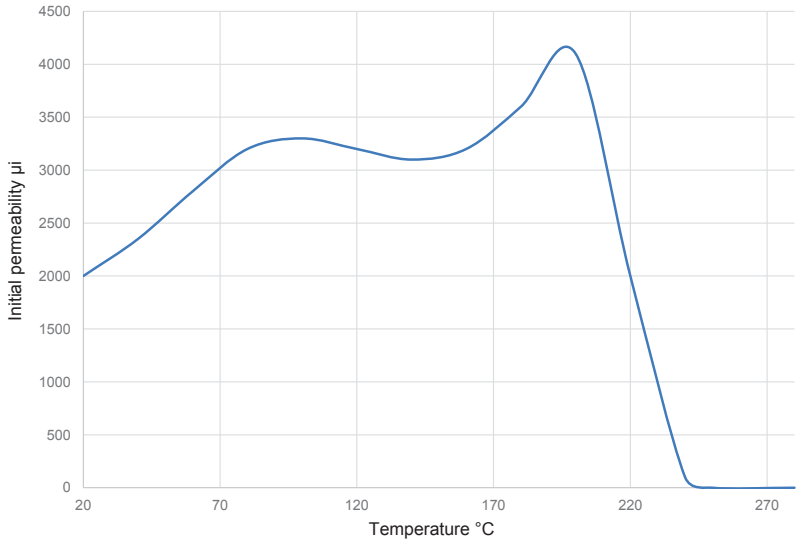


Figure 2.7: Initial Permeability μ_i versus Temperature for MnZn at $B = 0.25mT$

2.1.6 Ferrite Resistivity

One of the advantages of using ferrite materials is they have very high resistivity at high frequencies due to domain structure. The high saturation si-ferrite such as MnZn materials have $100-200\Omega/cm$, while it reaches $200-2000\Omega/cm$ for power si-ferrite. The ferrite resistivity depends on the frequency and temperature of operation. Usually the resistivity decreases with increasing temperature in the range of (0 to 40°) and decreasing frequency [47], while it increases with temperature growth over 40°.

2.1.7 Eddy Current Loss

When an alternating current passing through an inductor, it will stimulate a time varying magnetic flux ϕ around the inductor and through its core according to Faraday's Law of Induction [48].

$$\oint \vec{E} \cdot \vec{ds} = -\frac{d\phi_B}{dt}$$

The rate of change in the stimulated flux $\Delta\phi$ will generate an induced Electromotive Force (EMF) across the domains of core material. Because the grains have a specific resistivity R_g, it will allow a certain amount of current to pass through the bounded domains, that is known as eddy current as shown in figure 2.8.

The eddy current can produce power loss P_e that is dissipated as heat [49], the value of P_e power dissipation is a function of the value of magnetic flux density B and its rate of change or flux frequency f_s as

$$P_e = K_e \times B_m^2 \times f_s^2 \frac{A_c}{\rho}$$

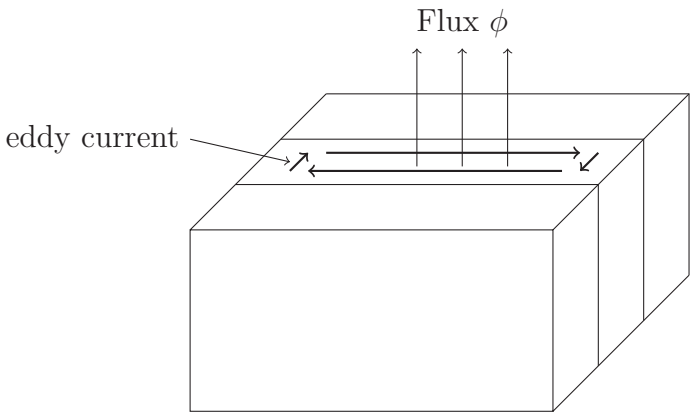


Figure 2.8: Eddy Current in Segments

Where A_c is the cross section area of the material and ρ is the resistivity of the material at a specific temperature.

2.1.8 Hysteresis Loss

All ferromagnetic materials are made of very fine grains; these grains respond when a magnetic flux strength is applied. Their responses will align all the domains in parallel to each other and directed to the applied magnetic flux.

If the flux direction or magnitude is changed or alternate, the domains should respond instantaneously to the rate of change, the delay in response is defined as hysteresis and it will cause a change in the $B-H$ characteristic of the material, as shown in figure 2.5. The delay in response will create residual flux $B_{residual} = \frac{\phi_{residual}}{A_c}$ and to element the effect of the residual flux, a current should be applied in the opposite direction as $H = \frac{N\ I}{L}$. The current will reduce the residual flux gradually until it reaches zero and this mean a certain amount of power is lost in the action [50].

$$P_{hyst} \propto f \cdot B$$

2.1.9 Fringing Factor F

Introducing a gap in cores is one of the methods to prevent saturation of soft magnetic materials. Unfortunately, gapping cores will lead to cause fringe flux around the air-gap. Consequently, fringing flux can impact the value of coil inductance, efficiency and it can cause extra loss because the flux will strike the windings and the core vertically.

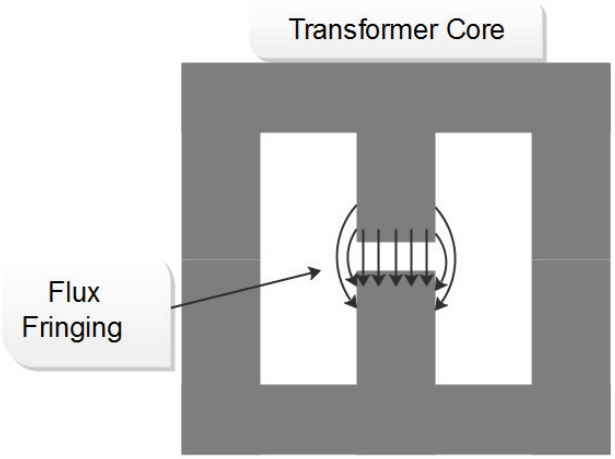
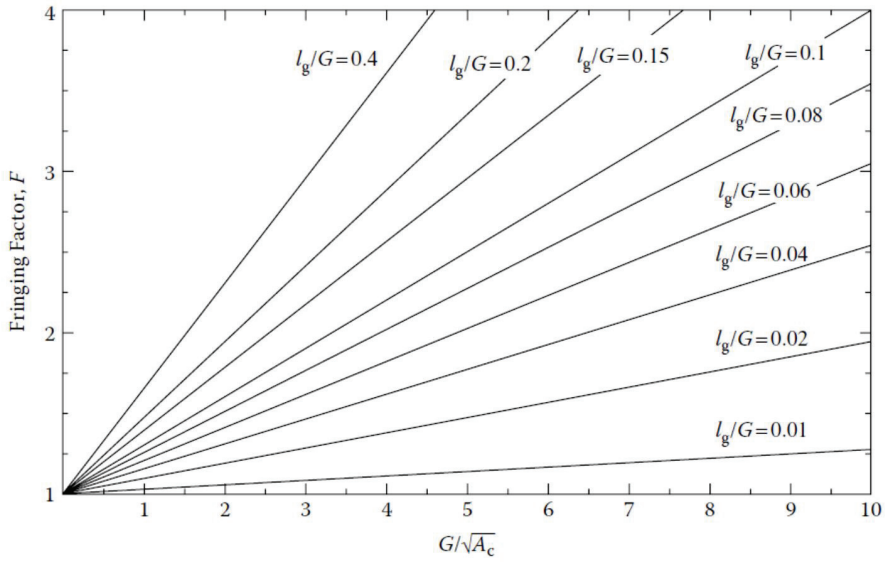


Figure 2.9: Flux Fringing Around Airgap

The previous figure 2.9, shows that the flux at the core edge can draw a non-linear path. Equation 2.1 can measure the fringing factor and it is always advisable to have $F \leq 1$.

$$F = 1 + \left(\left(\frac{lg}{\sqrt{A_c}} \right) \times \ln \left(\frac{2 \times l_W}{lg} \right) \right) \tag{2.1}$$



[45]

Figure 2.10: Increase of Inductance with Fringing Flux at the Gap

2.1.10 Skin Effect

At high frequency the magnetic field cannot penetrate into the interior of a solid conductor completely, this phenomena known as skin effect and it can be defined as " The degree of penetration of a conductor by magnetic flux and eddy current" [51].

Skin effect is affected by two factors, which are material resistivity and the operating frequency of the current. The general equation to find the skin depth is:

$$\delta = \sqrt{\frac{\rho}{\pi \mu_r \mu_o f}}$$

where μ_r is 1 and ρ for copper is 1.724×10^{-8} $(\Omega.m)$at $20°C$.

then

$$\delta = \sqrt{\frac{1.724 \times 10^{-8}}{\pi \times 4 \times \pi \times 10^{-7} f}}$$

$$\delta_{Cu} = \frac{66.08}{\sqrt{f}}$$

while ρ reached 2.3×10^{-8} $(\Omega.m)$ at $100°C$ at 50 Hz, which increases δ to 9.49×10^{-8} (m) as shown in figure 2.11 [51].

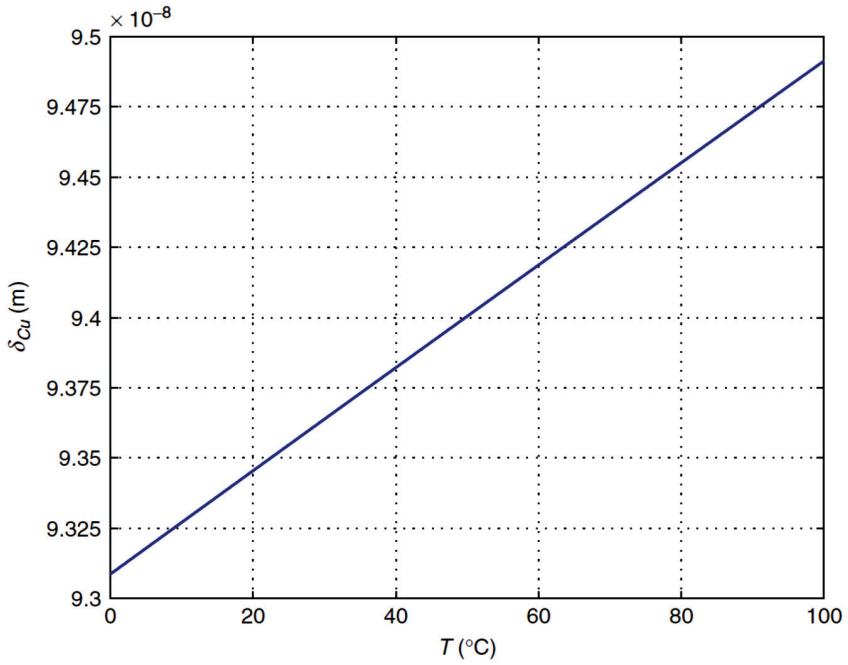


Figure 2.11: Skin Depth for Copper as Function of Temperature at 50Hz

2.1.11 Proximity Effect

Is a phenomena that affect two conductors carrying current and next to each other. When two conductors or more are carrying current, their magnetic fields may add or subtract. The effect of resultant field can cause non-homogeneous current distribution through the conductor surface area as shown in figure 2.12. Which can led to increase the conductor AC resistance significantly [51].

Distance between the conductors will affect the value of produced magnetic field and mainly there are four factors that affect the magnitude of proximity, which are:

1. Frequency.
2. Conductor geometry.
3. Arrangement of conductors or windings.
4. Spacing.

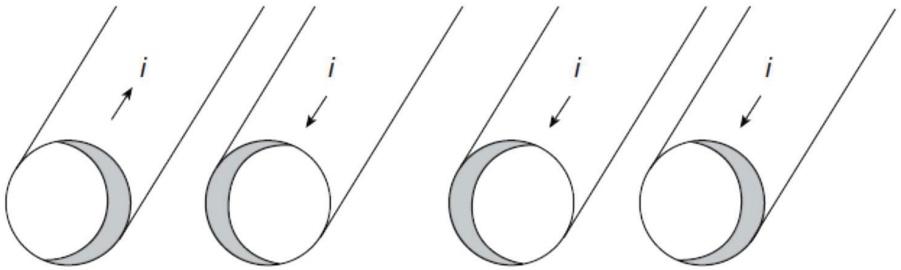


Figure 2.12: Proximity Effect in Two Conductors When the Current in Same and Opposite Direction

to avoid huge proximity loss, having a single layer of conductors in the transformer or alternating between primary and secondary windings is required, though it will not element the effect.

2.1.12 Effect of Core Gapping on Inductance

In power electronics converters, magnetic cores usually require gapping to avoid saturation or to reduce losses. Unfortunately, such action can leave an impact on coil inductance due to the changing of B-H characteristic of the core. Such a change in B-H curve is caused as a result of the difference in permeability between free space and magnetic material, as shown in figure 2.13.

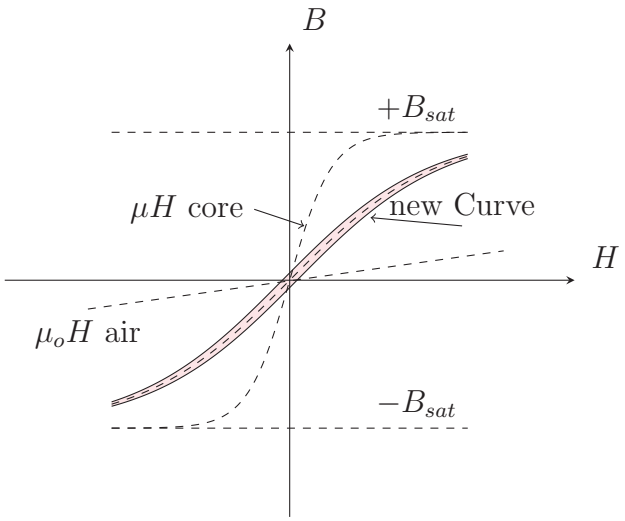


Figure 2.13: Effect of Core Gaping on Hysteresis Loop

From the previous figure, the line $\mu_o H$ is the flux density in the free air while μH is the flux density of the magnetic material. Introducing an air gap in the core will change the total reluctance as $\Re = \frac{l}{\mu A_c}$

$$\frac{l_{total}}{\mu_e A_c} = \frac{l_g}{\mu_o A_c} + \frac{l_c}{\mu_o \mu_r A_c}$$

and by assuming ($l_c >> lg$) then

$$\mu_e = \frac{\mu_o \mu_r}{1 + \mu_r \left(\frac{l_g}{l_c}\right)} \tag{2.2}$$

where μ_e is the effective permeability.

Consequent to the previous total inductance will be effected as

$$L = \frac{N^2 A_c \ \mu_e}{l_{total}}$$

$$L = \frac{N^2 A_c \left(\frac{\mu_o \mu_r}{1+\mu_r \left(\frac{l_g}{l_c}\right)}\right)}{l_{total}} \tag{2.3}$$

2.1.13 Synchronisation

Synchronisation is a method of aligning two waveforms such that they have the same frequency, magnitude and phase angle to each other. The synchronisation can be performed by monitoring the main waveform continuously in real time, while adjusting the secondary source to it. The failure of performing accurate synchronisation can cause a huge current transient through the secondary source that can lead to damage [52].

2.1.14 Zero Crossing Detector

This method is used to track or measure a system frequency. It relies on measuring the number of peaks per unit time or comparing the system voltage with a reference to indicate the starting point of a cycle. This method can be implemented digitally or using analogue systems. Its accuracy is subject to the period of measuring peaks and the measured signal quality [53]. Figure 2.14 shows a basic type of the detector, where the circuit generates a pulse at each zero crossing point of the rectified waveform.

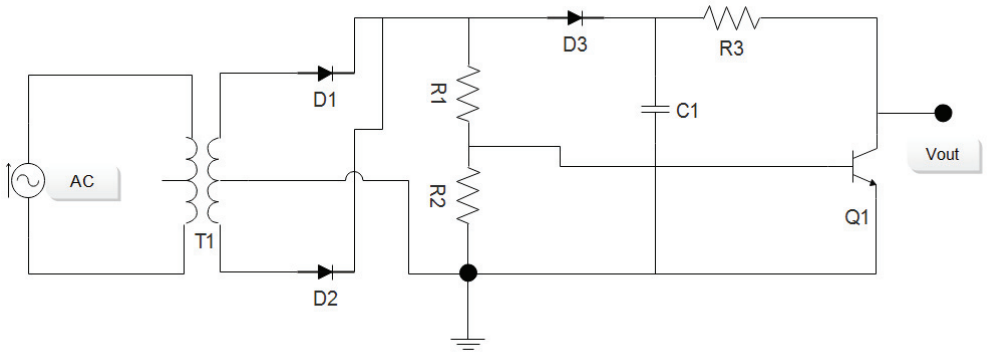


Figure 2.14: Basic Zero-Crossing Detector

2.1.15 Phase Locked Loop

The PLL is a time domain method used to track a signal frequency. Figure 2.15 represent PLL system, it uses a feedback to compare the generated output signal to the input. The arrangement can change the output waveform frequency by adjusting the internal oscillator [53].

- Phase detector: this block generates an output ε_{pd} that is relayed to the phase difference between PLL output and the input signal.
- Loop Filter: this block contains a low pass filter to elemental high frequency component form the AC source. This filter can be constructed ether using first order low-pass filter or PI controller.
- Voltage Controlled Oscillator: this block is responsible to generate the AC output, the generated signal frequency is a function of the loop filter block.

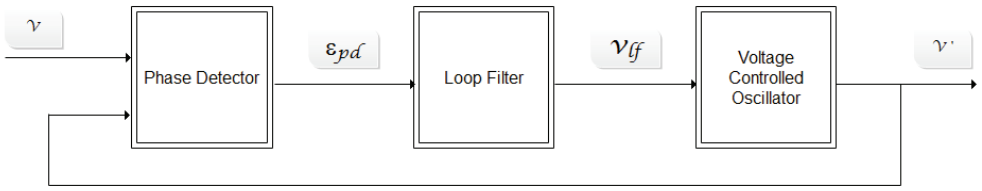


Figure 2.15: Basic Structure of a PLL

The elementary block diagram of the PLL is shown in figure 2.16. It can be seen that the phase detector is implemented using a multiplier, the LF is utilized the PI controller and the voltage controlled oscillator is consist of function supplier and integrator.

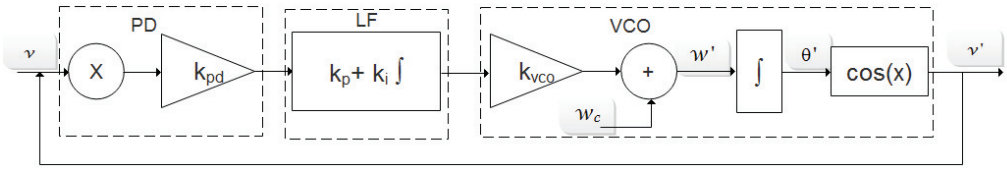


Figure 2.16: Block Diagram of an Elementary PLL

2.1.16 Fourier Analysis

The analysis was firstly introduced by the mathematician and physicist J.B Fourier in 1807 [54]. At the time his theory made a controversial statement that any continuous signal can be represented by a series of sinusoidal waveforms. The analysis is currently used in different application to transfer analogue signal into frequency domain.

This theory can be used with.

- Periodic continuous signal, is the signal that repeat itself periodically after τ of time.
- Aperiodic continuous signal, is the signal that does not hold a certain shape as it has a continuous change in magnitude and frequency with the time.

To find frequency components of a periodic waveform, multiplying the input signal by a the mathematical functions (sine and cosine) at different frequencies. The product of the cosine function by the input signal will result an odd set of frequencies, while the even set of frequencies can be obtained by multiplying the input signal by the sine function. On the other hand finding

the average of the analysed signal will represent the DC component within it.

Based on the previous, any signal can represent by Fourier expression, as follow.

$$v(t) = a_o + \sum_{n=1}^{\infty}(a_n \ \cos(n\omega t) + b_n \ \sin(n\omega t)) \tag{2.4}$$

The previous equation can breakdown into the main components, where the coefficients are determined by.

$$a_o = \frac{1}{T}\int_0^T v(t)dt$$

$$a_n = \frac{1}{T}\int_0^T v(t) \ \cos(nwt)dt$$

$$b_n = \frac{1}{T}\int_0^T v(t) \ \sin(nwt)dt$$

From the previous, each periodic harmonic can be represented as a vector $V_n' = V_n \angle \theta_n$.

Where

$$V_n = \sqrt{{a_n}^2 + {b_n}^2}$$

$$\theta_n = \arctan\frac{B_n}{a_n}$$

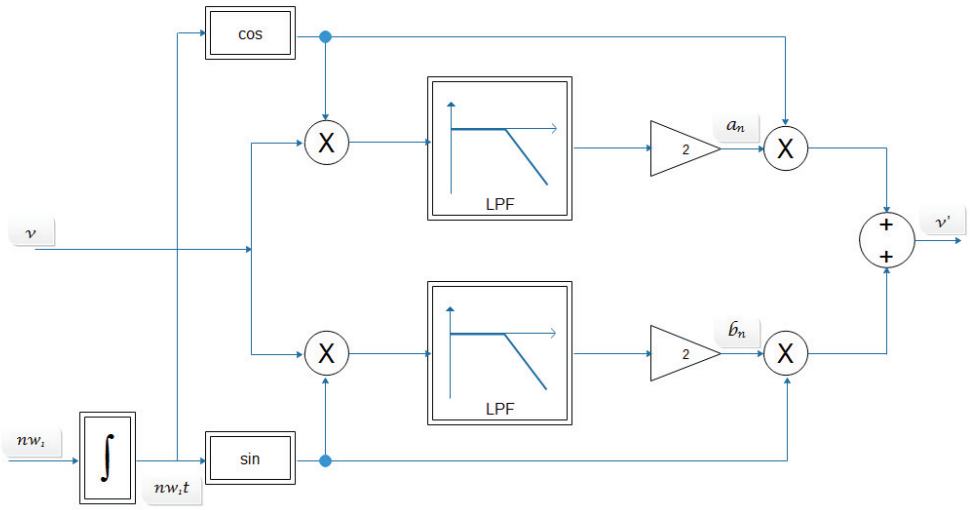


Figure 2.17: Adaptive Filter using Fourier Series

Figure 2.17, represent an adaptive filter by utilizing Fourier series. The mean value of the output is subject to the Low Pass Filter (LPF) that is set by the lowest frequency. Under normal operation the lowest frequency of the grid voltage matches the fundamental.

2.1.17 Discrete Fourier Transform

Is a tool that is used to convert time domain data into the frequency domain. The tool was developed due to the requirement of modern digital systems to analyse data. Analysing continuous waveform using a digital system requires sampling the signal to N number of samples, that what is making referred to the system as discrete [55]. To apply DFT to an analogue signal, there are two steps will be required to convert it into a digital signal.

- Sampling and Hold
- Quantization

Applying the previous steps to a continuous analogue signal can lead to loss information as it will be discussed.

2.1.18 Sampling Theorem

Is a procedure that is followed to convert continuous signal into digital, the procedure can be performed by chopping the analogue signals to samples with intervals of $\frac{1}{T_s}$ as shown in figure 2.18. These samples will hold some of the information of the analogue signal. To ensure that the data in the samples are enough to reconstruct the analogue signals with minimum losses, the switching frequency, $F_s \geq f_{analogue}$ this rule is known as Nyquist condition. Choosing a lower switching frequency F_s or under-sampling can lead to loss of information that is known as aliasing [56, 57].

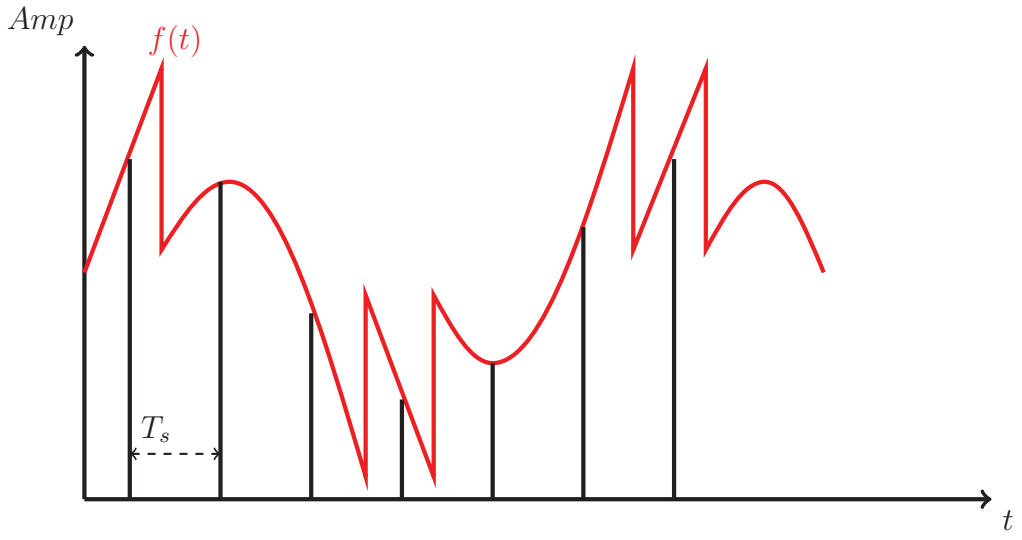
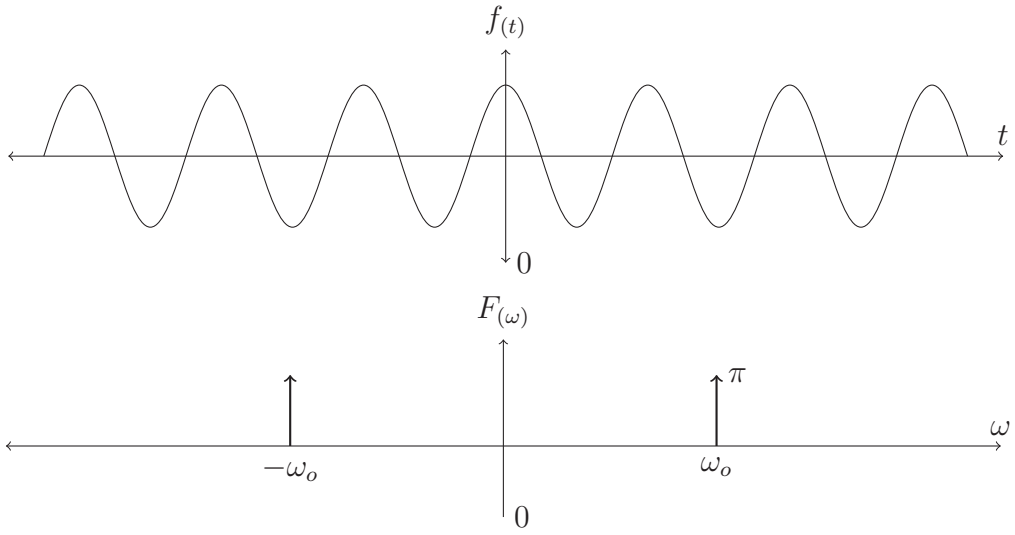


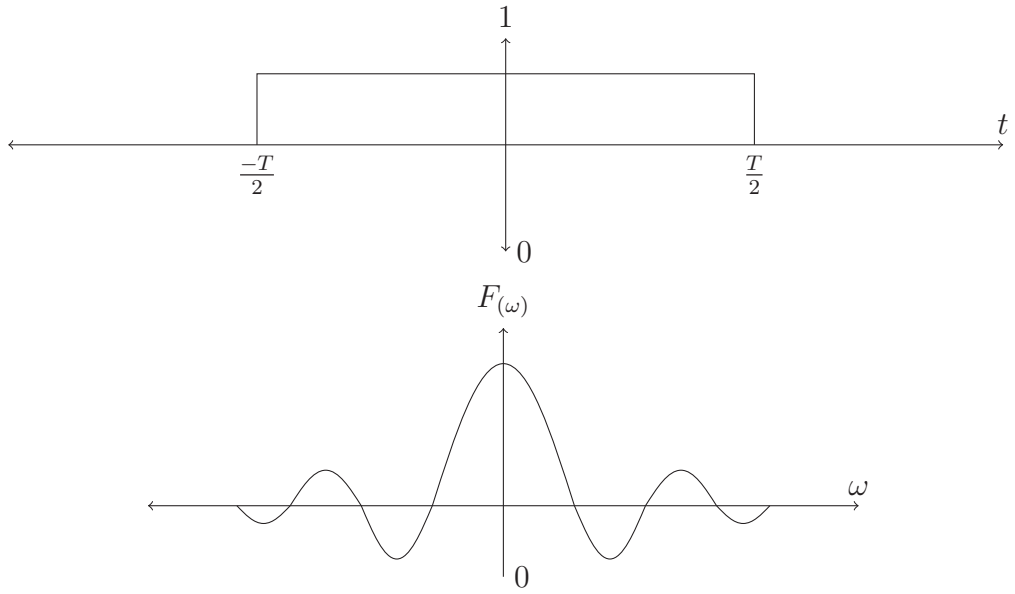
Figure 2.18: Sampled Analogue Signal

2.1.19 Window Function

To apply DFT for a continuous periodic signal, truncation of the input signal is required as it will reduce the spectrum leakage. It can be performed by multiplying the input signal figure 2.19a by a windowing function with limited width 2.19b, the resultant waveform will be a sample of the continuous periodic signal but with limited window width as shown in figure 2.20 [57,58].



(a) Sine Wave and its Spectrum



(b) Windowing Function and its Spectrum

Figure 2.19: Different Waveforms Spectrum

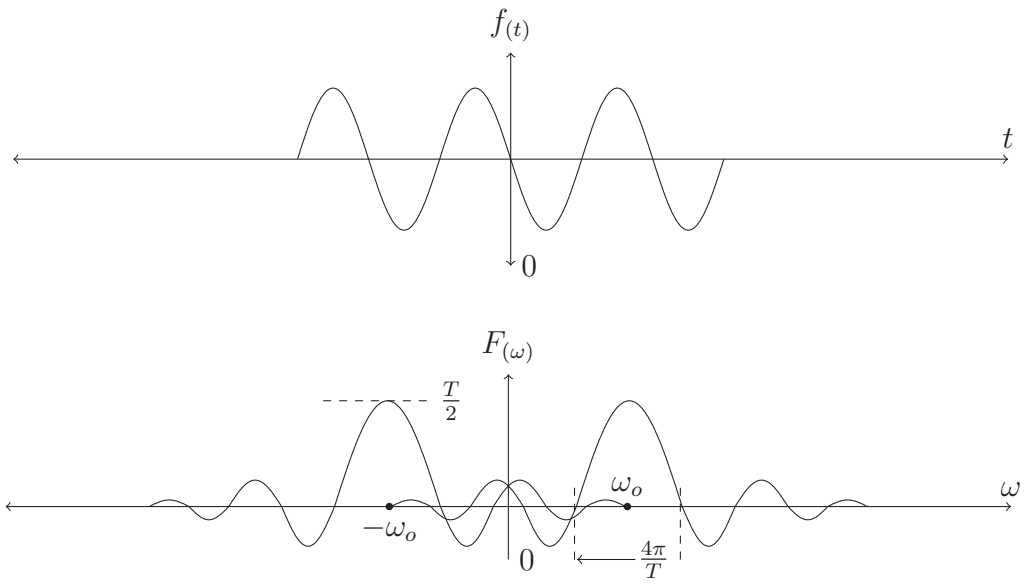


Figure 2.20: Truncation Sinusoidal Waveform and its Spectrum

The resultant waveform with finite in time domain will produce a function that has a spectrum of two *Sinc*s' placed at ω_o and $-\omega_o$.

Unfortunately, if the continuous input signal has unknown frequency, then there is a possibility that the window width may differ than the period of one cycle. This will cause truncation of non-integer number of cycles. Such a condition can lead to have a wide band of noise that can affect by overlapping the frequencies at both ω_o and $-\omega_o$ as shown in figure 2.21 which is known as spectral leakage. Where spectrum of the *Sinc* function at ω_o will spread to interact with the $-\omega_o$ causing a change in the magnitude of both $\pm\omega_o$.

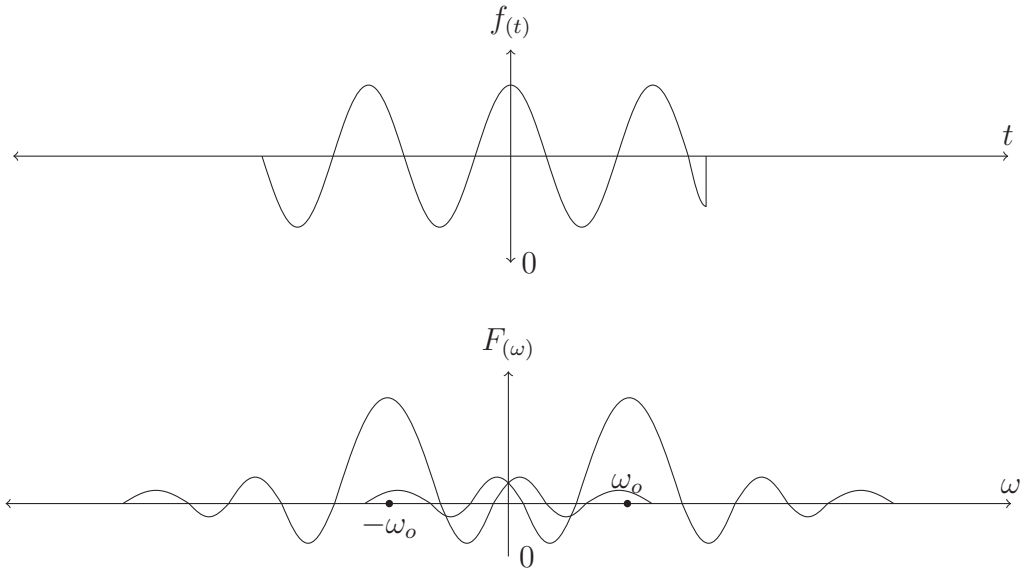


Figure 2.21: Unmatched Window Truncation Waveform and its Spectrum

The previously discussed condition can be one of the DFT drawbacks though there are some research that offer solutions for such condition such as using variable window width.

2.1.20 DFT weakness

The DFT has five weakness points that can be described as follows:

Computational load to execute the DFT there are several additions and multiplications that should be performed which required huge time to apply. For clarification the 1024 samples will require 4 million additions and multiplications [55].

Where the number of additions $= M(2M + 2(M - 1)) = 4M^2 - 2M$

multiplications $= M(4M) = 4M^2$

Error due to Quantization Noise Quantization is a process that follow

the sampling, where samples magnitude should change into a digital value. The process is limited by the number of bits that the ADC is having, it is known as resolution. Therefore the lower resolution can cause higher difference between the signal real magnitude and the digital level and vice versa. Therefore the quantization process will always lead to some loss of the information as shown in figure 2.22. That error is defined as the signal to quantization noise error SQNR

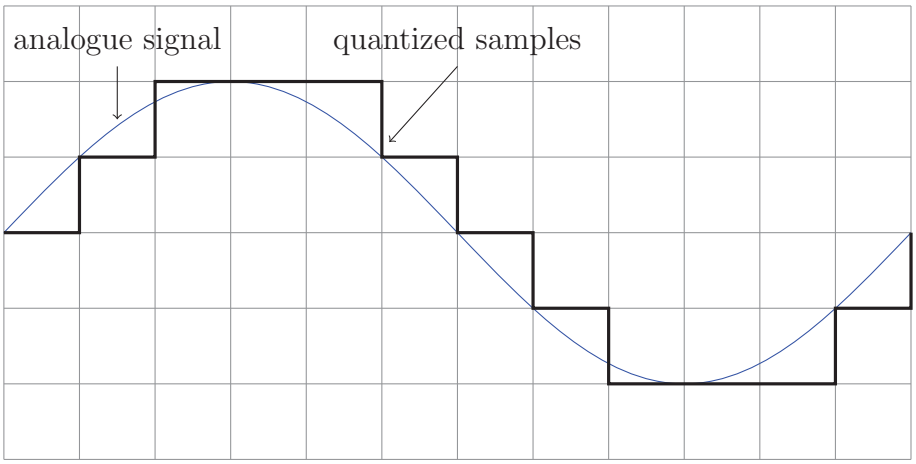


Figure 2.22: Sampling and Quantization of Sinusoidal Waveform

High Sidelobes , When the window function is narrow that will generate a wide spectrum of noise. Usually the truncated signal has a zero value everywhere except $\pm\omega_o$, but this is not the case due to the sidelobe caused by spectral leakage. The sidelobes have a peak magnitude of 13.3dB the peak of the main lobe, while the decay rate is $\frac{1}{\omega}$, which is -6dB.

Signal Transient the DFT has a bad response to signal transient as it requires an infinity periodic waveform. Transient can cause spreading noise along the spectrum leading to loss the ability to find the funda-

mental frequency. Likewise, it and can cause a non-stationary statistic which can effect on the average of the signal. Figure 2.23 shows, two sinusoidal waveforms that have the same DFT mathematical result.

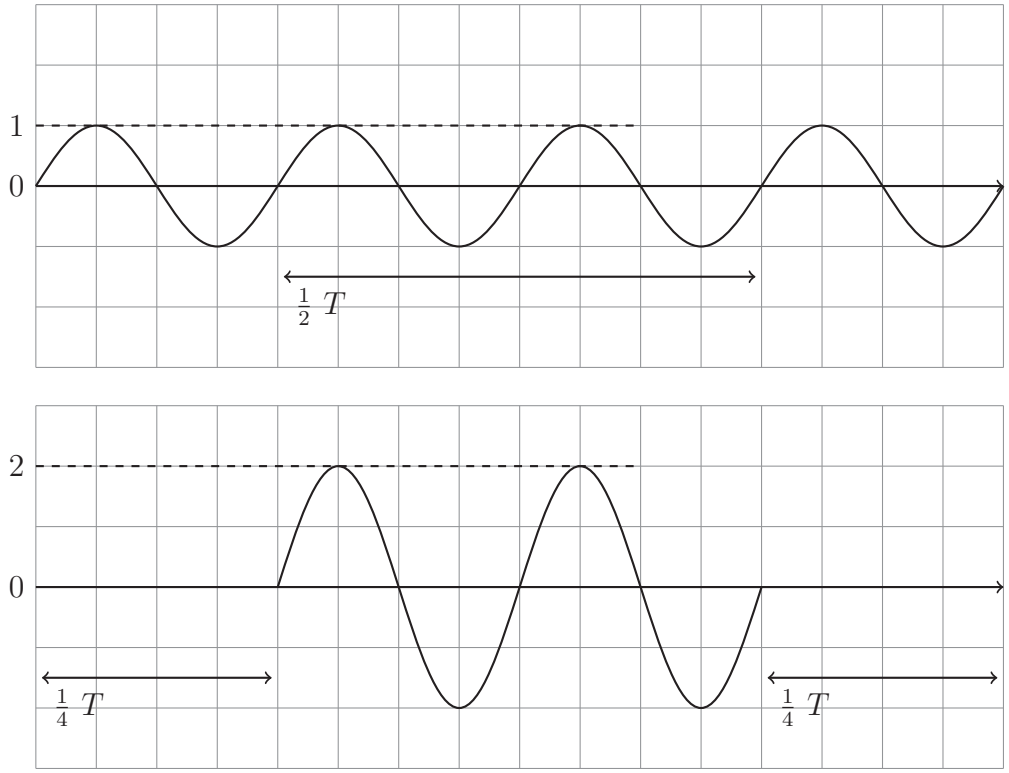


Figure 2.23: Two Sinusoidal Waveform That has the Same DFT Value

Frequency straddle loss is the reduction of DFT output due to the input frequency shift. Where frequency shifting will create an error in DFT due to the mismatch between the filter frequency bin of the DFT and the input waveform.

2.2 Distributed Generation Function

According to [38], When Grid connected inverter operates as a part of DG, it usually operates independently of dispatch centre. This type of operation can make DG have a big impact on the performance of the network, which obligate inverter manufacturers to follow grid requirements in order to produce inverters that can feed the grid, such as: [53].

1. Synchronising and paralleling
2. Power source transfer
3. Metering and monitoring
4. Electrical protection
5. Power conditioning and conversion

Two of the previous can contribute in huge impact to the efficiency, which are power conversion and synchronisation.

2.2.1 Power Conditioning

Delivering energy from a source to grid in DG, requires using of multi-stage or cascaded converters. There are various types of DC voltage boosters that can be used to raise the source voltage and make it suitable to grid rating, the basic types of the converter can be listed as:

- Boost converter.
- Buck - boost converter
- Interleaved boost converter.

- Forward converter with boosting turns ratio.
- Flyback converter.
- C'uck converter.

Form previous, all non-isolated DC converters can be classified according to the topology of operation as shown in figure 2.24.

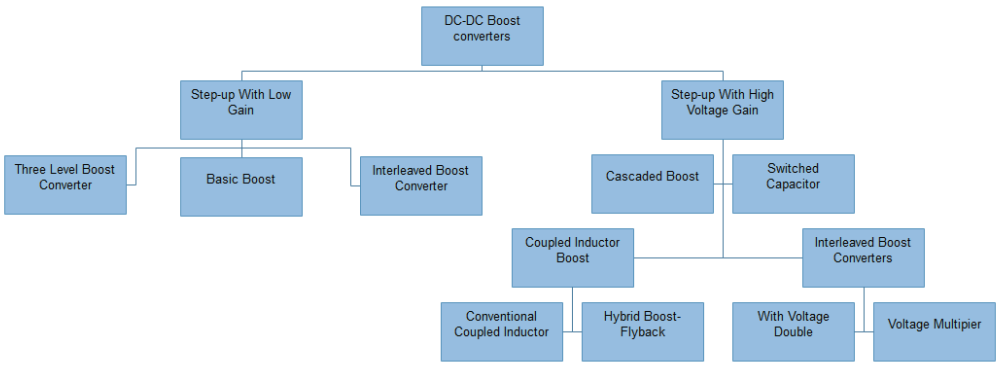


Figure 2.24: Classification of Non-Isolated DC-DC Boost Converters

Practically, the main factors that determine using a converter from the previous list are efficiency, power handling capability and the ability to operate with continuous variable duty cycle or frequency.

Because the proposed converter can be considered as an interleaved boost with multiplier, both principles of operation of both interleaved and basic boost will be covered in this chapter.

Boost Converter

One of the methods that can be used to step-up source voltage is by using Boost converter [59] shown in figure 2.25. The converter has a minimum number of components and can provide decent efficiency at low duty cycle.

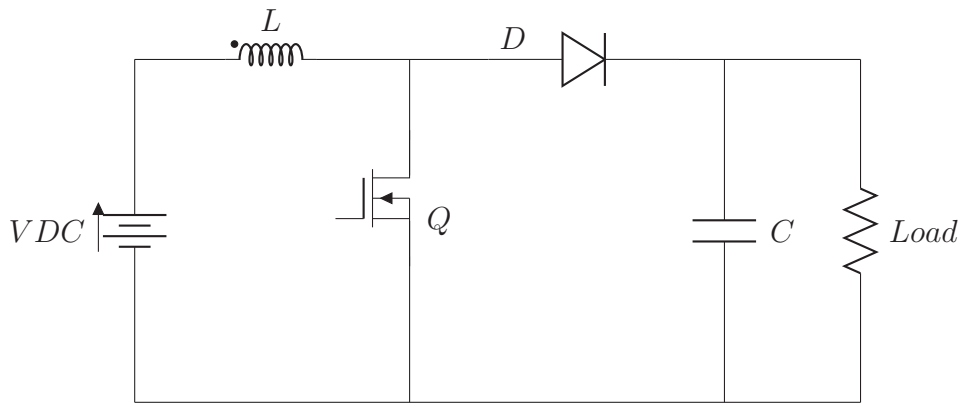
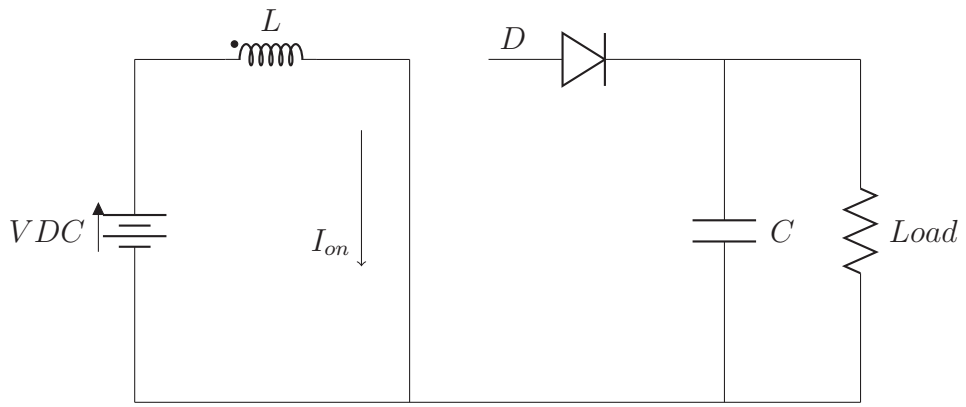
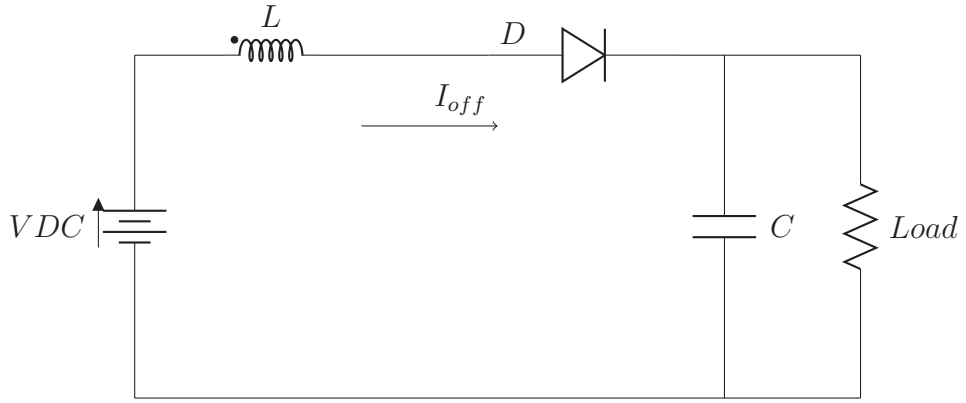


Figure 2.25: Boost Converter

The circuit starts to operate when the MOSFET is closed, a flow of current will pass through the inductor L leading to energise the inductor. Because the capacitor C holds the output voltage value, it will switch the diode to reverse bias. Switching the diode to reverse bias will prevent the capacitor to discharge through the MOSFET as shown in 2.26a.



(a) During on Time



(b) During off Time

Figure 2.26: Boost Converter Operation

When the MOSFET is off, the inductor L will de-energise through the diode to feed the load and the capacitor C as in figure 2.26b.

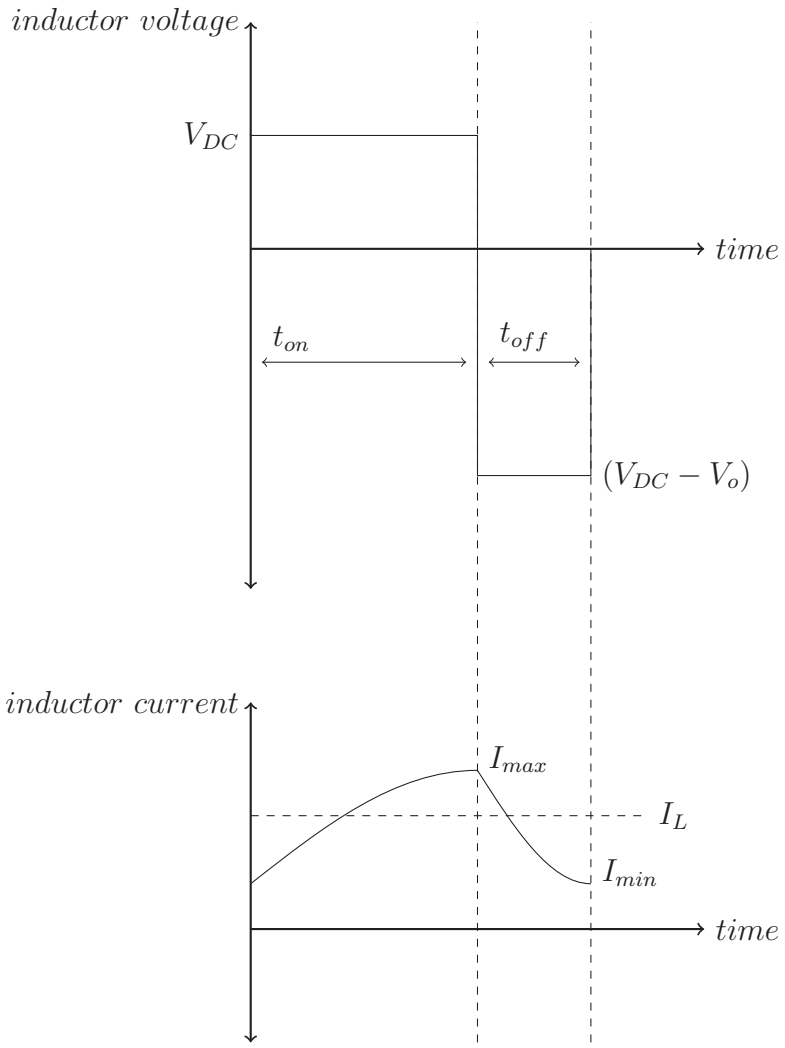


Figure 2.27: Boost Converter Waveforms

The output voltage will be

$$V_{DC} \times t_{on} + (V_{DC} - V_o) \times t_{off} = 0$$

by dividing both sides by the switching time period T_s and assuming the

circuit is lossless

$$T = t_{on} + t_{off}$$

$$\frac{V_o}{V_{DC}} = \frac{T}{t_{off}} = \frac{1}{1-D} \tag{2.5}$$

It can be seen from 2.5 equation, to obtain higher voltage gain, the duty cycle should be very big which will require a huge time to energise the inductor.

to find the I_{max}

$$I_{max} = \frac{V_{DC}}{r_i}(1 - e^{\frac{-r_i}{L}t})$$

During the off time the current will feed the load according to

$$I_{min} = I_{max} \times e^{\frac{-r_i}{L}t}$$

Tapped Inductor Boost Converter

The converter was firstly presented by [60], this type of converters shows in figure 2.28 is relying on two factors in voltage boosting, the difference in the number of turns between the coils, as they will act as a transformer, and duty cycle.

The operation of the tapped inductor is similar to the basic Boost topology, when the MOSFET is closed a current will pass through L_1. As both L_1 and L_2 are mutually connected, certain potential difference will be produced across L_2 when the MOSFET is ON and the voltage source is connected across the L_1 inductor. During ON state the diode will be in reverse bias and there is no current feeding the load and both inductors will act as storage energy elements.

When the MOSFET is open, the inductors L_1 and L_2 will de-energise through the diode to feed the load. According to the mode of operation and

the mutual effect of the inductors, the output voltage will be subject to the ON time of the MOSFET and the turns ratio of the inductors. During this state the diode will be in forward bias and current will flow to feed the load.

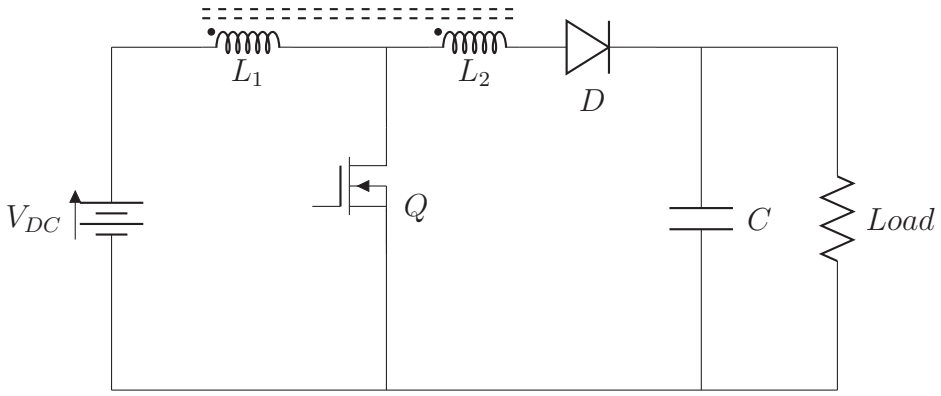


Figure 2.28: Tapped inductor

Voltage gain for this converter can be obtained by [60]

$$\frac{V_o}{V_{DC}} = \frac{1 + (\eta \times D)}{1 - D} \tag{2.6}$$

where η is the turn ratio, D is the duty cycle.

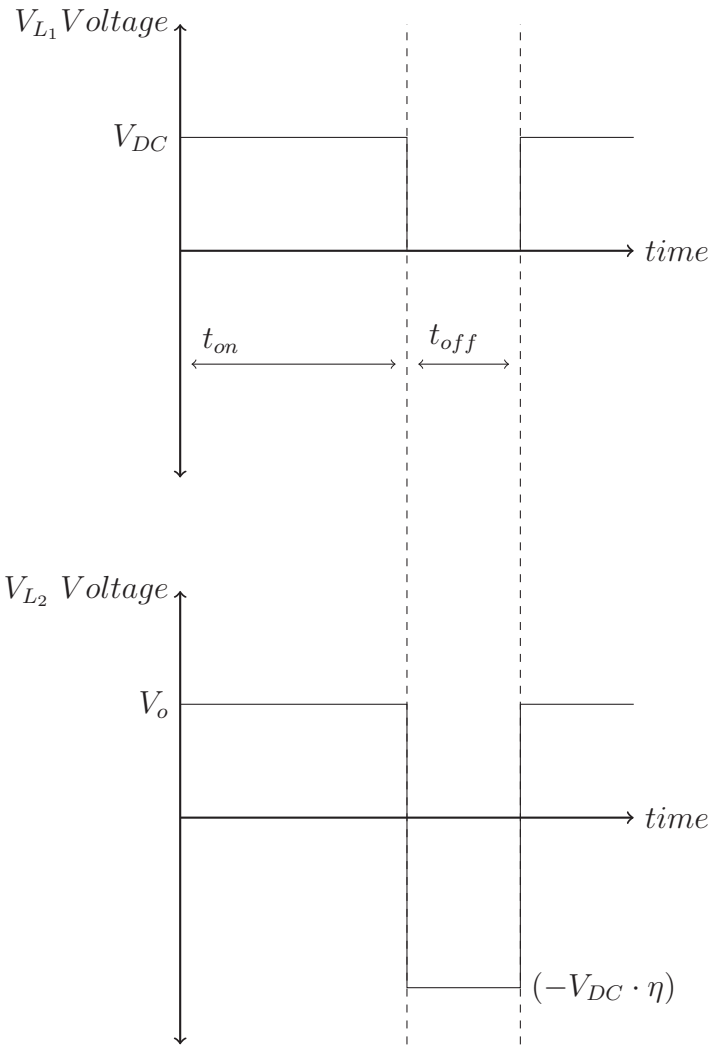


Figure 2.29: Tapped Boost Inductor voltage

Interleaved Boost Converter

Connecting two or more boost converters can be one of the solutions to increase power handling capability and it contribute in reducing the ripple factor of the input current. Paralleling boost converter as shown in figure 2.30 was improved later by integrating the inductors in one magnetic circuit. The integration helped to reduce the number of used magnetic components

and increased the output power even further [11]. Likewise increasing the number of parallel connected converters will increase the gain even further.

The circuit operates when Q_1 and Q_2 is closed, current will pass through the switches and energise the inductors L_1 and L_2, both D_1 and D_2 are in reverse bias. When Q_1 is closed and Q_2 is open, huge voltage will appear across L_1, which make D_1 in forward bias, which will allow the current to pass and feed the load. When both Q_1 and Q_2 are ON during the overlap period, the flux produced form the first inductor L_1 will eliminate the flux of the second inductor L_2 because they are connected in reverse order. This mode of operation will required an extra input inductor to prevent short circuit the voltage source.

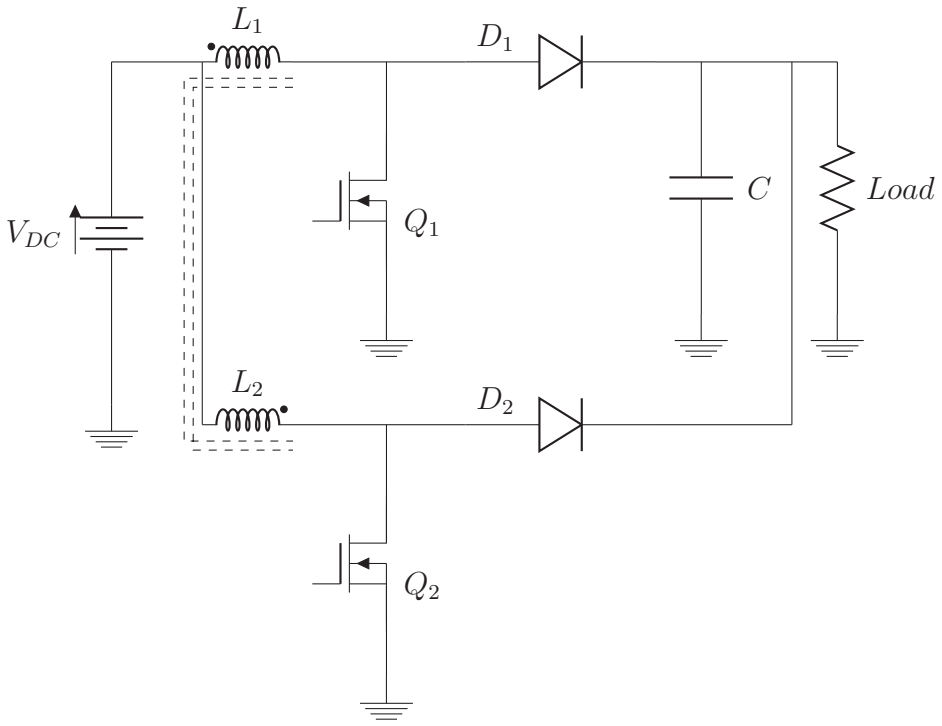


Figure 2.30: Interleaved Boost Converter

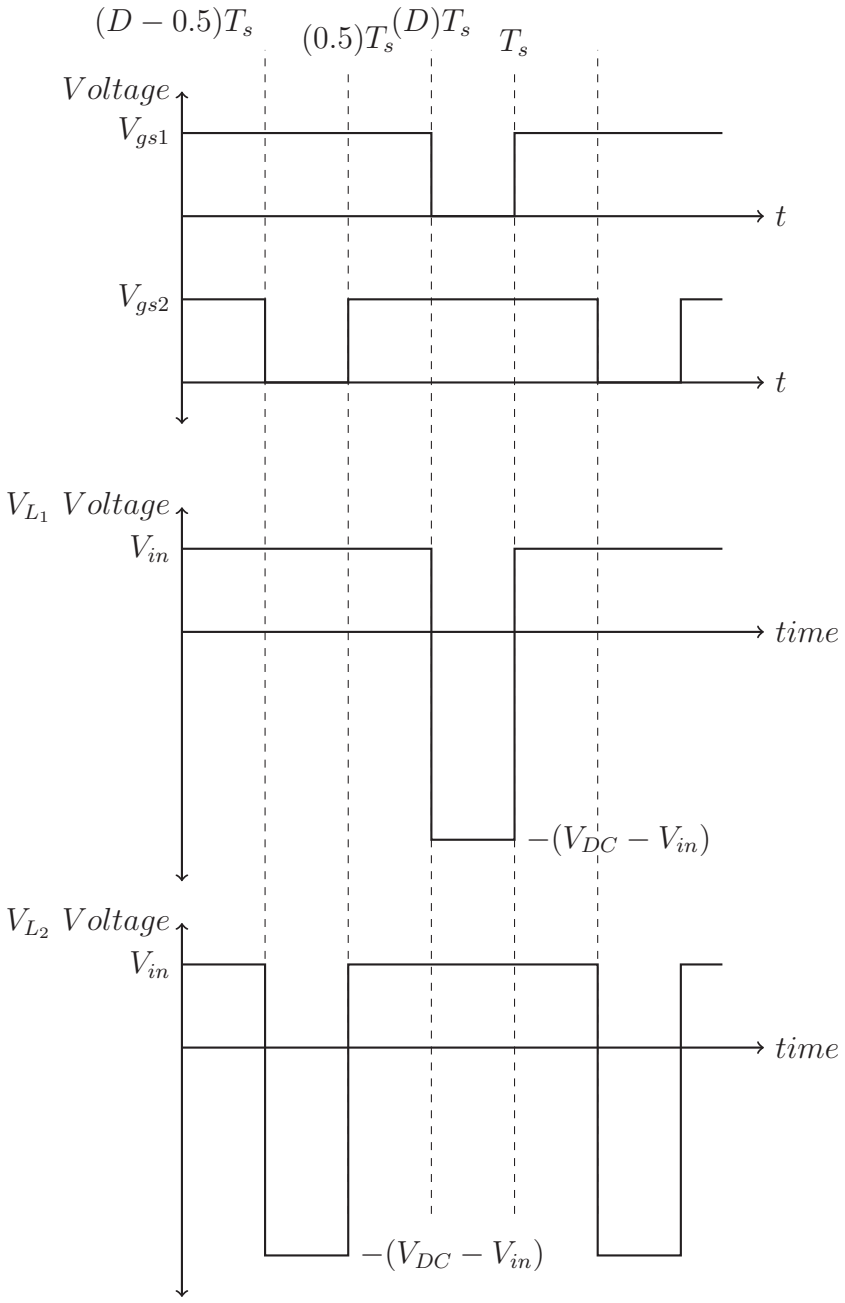


Figure 2.31: Tapped Boost Inductor voltage

The only one factor that effects the voltage gain for this topology is the duty cycle and the voltage gain will be similar to the conventional boost converter gain, but multiplied by a factor of $(1 + D)$ [11].

$$\frac{V_o}{V_{in}} = \frac{1 + D}{1 - D}$$

Where D is the duty cycle or the time required to energise inductor.

2.3 Magnetic Components

Using a magnetic component in power electronic converters can make it act ether as a storage element or high coupling coefficient material, Which is combined with provide ground isolation and change in voltage ratings by controlling *volt/turn* ratio of the windings. The importance of this material was a key to improve the technology of producing ferromagnetic materials for high frequency applications.

The purpose of using ferromagnetic materials to construct a magnetic element in converters, is to use the advantage of having high permeability characteristic to provide a low reluctance path for the flux to construct. This should reduce the leakage flux which can lead to improve the coupling between windings of a transformer or coupled inductors.

2.3.1 Types of Magnetic Materials

Magnetic materials and cores can be classified according to their purpose of use or depending on their ability to store energy. Materials such as powder iron, Permalloy powder and Kool Mμ can store a considerable amount of energy, therefore these materials can be used to form filter inductors in SMPS applications. Such materials have a permeability of 15 to 200 that requires high magnetization current which make them not suitable to be used in forming transformer [61].

On the other hand ferrite and ceramic materials that are made of manganese, zinc and nickel such as MnZn si-ferrite. These materials have a permeability of 1500 to 3000 and can operate at frequencies up to 1 or $2MHz$. Because of high permeability these materials will cause low magnetization current and because of the high frequency operation characteristic, it makes

them suitable for forming power transformer in SMPS. Ferrite and ceramic cores has low saturation flux density B_{sat} in comparison to powder iron, which can be considered as a disadvantage and a limiting factor during the design. Another disadvantage is related to ferrite is less robust which makes it fragile to shock and limiting its use in automotive application.

2.3.2 Core Selection

After choosing a suitable material, selection of core shape is the second step. Magnetic cores are selected depending on different factors as shown in table 2.2.

	Core Cost	Bobbin Cost	Winding Cost	Winding Flexibility	Assembly	Mounting Flexibility	Heat Dissipation	Shielding
Pot Core	high	low	low	good	simple	good	poor	excellent
PM Core	high	medium	low	good	simple	excellent	medium	excellent
E Core	low	low	low	excellent	simple	good	excellent	poor
EC Core	low	medium	low	excellent	medium	fair	good	poor
Toroidal	low	none	high	excellent	hard	poor	good	good
PQ Core	high	high	low	good	simple	fair	good	fair

Table 2.2: Different Cores Characteristics

there are other factors that can affect the selection, such as leakage flux, footprint, size and profile of the core. Some of the cores have other factors as it cannot handle large conductors or it is not available in big size such as pot core.

Toroidal cores can perform in an acceptable way during the tests for prototypes as it offers flexibility to increase power handling capability by paralleling cores through stacking two or more to each other. Where this flexibility is not available among other types of cores such as RM, PM and PQ. However, using toroidal cores can cause huge amounts of leakage flux in comparison to other cores because it does not provide shielding.

Regarding heat dissipation, all core can perform well in this area, excluding pot cores, PQ and PM cores. However, if the amount of heat is controlled by keeping the dissipation at low level, it will leave a positive impact as the core iron loss is inversely proportional to temperature.

There are some other shapes such as RM, E I, ETD and EE as different companies produce different shapes. From the previous, main criteria to select a core shape can be varied according to designer preference such as cost or shielding or heat dissipation.

2.3.3 Transformer Design Consideration

Designing a transformer for such a converter requires great care, where all windings should be distributed evenly across the core in order to prevent residual flux accumulation, as it will discuss later. On the other hand, uneven coil distribution will cause a difference in the switching current, leading to an extra ripple in the input and causing a DC bias around the core hysteresis loop of the transformer core.

Operating the core with low flux density by having a small gap of $0.1mm$ with low fringing will help to reduce the effect of the residual flux accumulation and will lead to a reduction in iron losses.

$$\frac{\int V \cdot dt}{NA} < B_{sat}$$

The number of turns of the primary windings for a non-gapped transformer core can be calculated by

$$N = \frac{V_{in}}{4 f_s B_{max} A} \tag{2.7}$$

Previous equation (2.7) can be used for a non-gapped core, but when a small gap is introduced, the winding inductance will be reduced, leading to a mismatch in transformer impedance causing a higher current magnitude to pass through the primary that may lead to saturation. However, to avoid the effect of the core gapping, the primary number of turns will be calculated based on the inductance value prior to introducing the gap.

The standard equation for inductances is

$$L = \frac{\mu A N^2}{l} \tag{2.8}$$

where L is the inductance, μ is the permeability, A is the cross-sectional area of the core and l is the magnetic path length (the mid-core circumference for

toroidal cores). μ shown in equation (2.8) is the absolute permeability of the inductor and is comprised of μ_0 (the permeability of free space) and μ_r (the relative permeability of the magnetic material).

$$\mu = \mu_0 \mu_r$$

μ_0 has a constant value of $4\pi \times 10^{-7}$H/m.

During the design, avoiding saturation is very important as it can occur for two reasons:

- When the produced flux density exceeds the value of B_{max} of the core ($0.5mT$ for N87), ie. when the current magnitude passing through the windings produces a Magneto Motive force ($N \cdot i$) value that exceeds the operation point μ as shown in figure 2.5.

  Where

  $$B = \mu H$$
  $$B = \mu \frac{N \cdot i}{l}$$

- Due to the flux accumulation in one direction of the $B - H$ curve when there is a DC component in the current waveform or when there is a continuous changing in the operating frequency.

At this point the material cannot support the magnetic characteristics and the winding will behave as a short circuit.

On the other hand, materials with lower permeability have a higher reluctance to the magnetic field, but will require more turns to achieve the target flux density. Such cores can operate at lower frequencies and switching losses can be reduced, however it will produce high copper and iron losses due to its large size.

Another factor that can affect the performance is the heat distribution caused by the windings. To ensure even heat distribution across primary and secondary turns, current density J should be the same or has the close value for both windings.

$$J_{prim} = J_{secon}$$
$$\frac{I_{prim}}{A_{prim}} = \frac{I_{secon}}{A_{secon}}$$

Though it is preferable to use higher cross section area than the calculated in the secondary winding to reduce losses and improve voltage regulation.

2.3.4 Transformer Power Capability

To achieve the high efficiency target, the transformer is optimized to have minimum copper and iron losses. Core selection is mainly based on physical size and inductance, where higher inductances are preferred to achieve a lower number of turns. However, small volume cores cannot have a high inductance, leading the design to have higher turns which means higher copper loss and less iron loss. The design optimization is to find a point where both losses have the same value by taking into consideration the core power handling capability and mechanical limitation that can be obtained by equation 2.9 [51].

$$W_a A_c \geq \frac{Po \cdot C}{B_m \cdot f_s \cdot 0.85} \tag{2.9}$$

where W_a is the window area of the core, A_c is the core cross section area, P_o is the total power carried by the core and C is a constant that varies depending on the core type and waveform shape.

$C = 5.07 \times 10^{-3} cm^2/Amp$ (square wave) for pot and E-U-I cores

2.3.5 Transformer Losses

There are different factors that affect loss values, such as:

- Operating frequency
- Core size and material
- Flux density
- Operating temperature

At higher frequency there is another effect which will appear across the boundary layers between the domains. This effect will be presented as a capacitance C_b. This will cause an extra loss in the material because of shorting the layer [62] at high frequency.

The slow response of the domains to flux changing can cause another type of loss in the core as hysteresis because it will require more energy to force the segment to change polarity. Both components are iron losses and are subject to the core size, core material, frequency and waveform shape at constant temperature.

$$P_e = K_e \cdot f_s^2 \cdot B_m^2 \cdot \frac{A_c}{\rho} \tag{2.10}$$

$$P_h = K_h \cdot f_s^x \cdot B_m^y \tag{2.11}$$

Where K_e and K_h are the eddy current and hysteresis constants, A_c is the material cross section area, while x is $(1 > x > 2)$ and y is $(2 > y > 3)$ the chosen values are 1.64 and 2.68 respectively, these values were selected depending on the operating temperature of the material N87 [63, 64].

There is another sort of power loss due to remanence or residual flux [65], and it can be considered as a constant at specific operating temperature. If the operating temperature is changed, then the residual flux value will

change because of the relaxation effect, where the system will move to new thermal equilibrium.

In the proposed method, the shape of current waveform will be considered as a factor which affects iron losses.

2.4 Power Inversion in DG

Increasing grid diversity by connecting different type of loads and power sources in parallel made the synchronisation process more challenging due to waveform distortion. Calculating the signal time accurately to switch the source ON to the grid can play a major role on micro-inverters, such as controlling produced losses and islanding detection because it can control over the produced power and grid quality.

Decreasing the waveform quality can lead to increase harmonics, which can reduce the reliability of the micro-inverter.

There are many techniques that can be used to perform phaser synchronisation, such as using PLL [29], Zero Crossing Detector, DFT in digital systems and modified zero crossing detector [30]. Generally, digital PLL is low in reliability when there is a DC component in the grid waveform, as the system saturate and losing lock [31]. On the other hand zero crossing detector cannot estimate the fundamental if the grid signal contains harmonics. Therefore, DFT is becoming widely used in analysis of fundamental component and harmonics of electric utility voltage and current [32].

Basically healthy grid voltage is a single tone waveform and it can be represented as

$$V_g = V_m \cdot \sin(\omega t + \theta_h) \tag{2.12}$$

If the grid waveform is distorted, then Equation 2.12 can be rewritten to

contain the sum of fundamental and odd harmonics

$$V_g = V_{dc} + \sum_{h=1}^{h=\infty} V_m \cdot \sin\left((h \cdot \omega t) + \theta_h\right) \tag{2.13}$$

Where h is the order of odd harmonics

In order to perform grid synchronisation, there are three variables as in equation 2.12, which are the fundamental voltage magnitude Vm, frequency ω and phase θ that should be measured precisely.

2.5 Methods of Synchronisation

Finding zero crossing point of the grid waveform is essential due to the effect of synchronisation on the delivered power (active and reactive), which will impact the total power delivered and stability.

There are different methods to perform the task

- Zero Crossing detector.
- Phase Locked Loop.
- Synchronisation using the Fourier Analysis
- The Discrete Fourier Transform.

A new approach based on using RDFT tool with linear approximation is presented, which will provide a computation reduction and high accuracy while tracking fundamental frequency in distorted grid waveform during synchronisation.

2.5.1 Discrete Fourier Transform

In digital signal processing, DFT is an essential tool that can be implemented to obtain the fundamental of a signal parameters by filtering out unwanted harmonics and it can be described as follows.

$$V_k = \sum_{n=0}^{M-1} v_n \cdot e^{-j2\pi n \frac{k}{M}} \tag{2.14}$$

where $k = 0, 1, 2, \cdots, (M-1)$;is Fourier Transform bin

M: total number of the samples taken at a sampling frequency.

v_n: the sampled voltage

Referring to the equation 2.14, DFT operates by sampling the input signal V_n by the switching frequency f_s to calculate the component of certain grid frequency (f_g). Bin-width or frequency resolution can be found by stating the number of samples (M) as shown in figure 2.32.

where:

$$binwidth = \frac{f_s}{M} \tag{2.15}$$

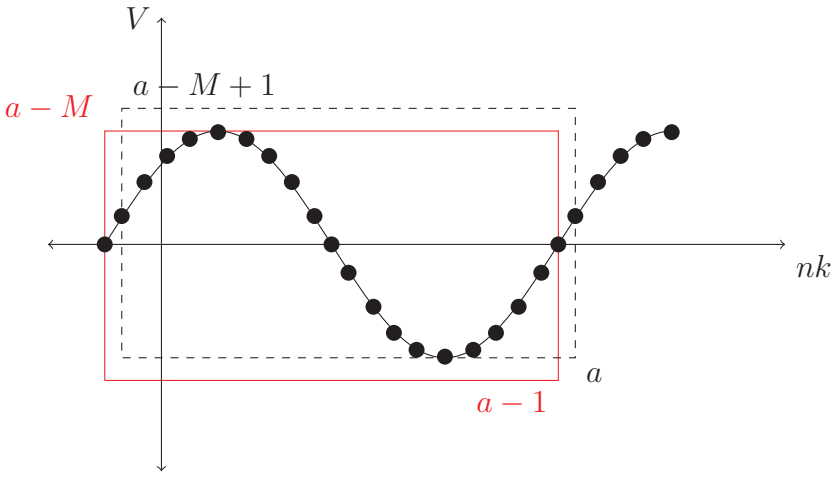


Figure 2.32: Sampling Window Width

The grid waveform in equation 2.12 can be rewritten in complex notation as follow [32]

$$\overline{V} = Ve^{-j\theta} = V\cos\theta + jV\sin\theta \tag{2.16}$$

By substituting the equation 2.16 in 2.14, the voltage phasor can be represented as real and imaginary component as follows:

$$\Re_e V[k] = \sum_{n=0}^{M-1} v_n \cos\left(2\pi n\frac{k}{M}\right) \tag{2.17}$$

$$ImV[k] = -\sum_{n=0}^{M-1} v_n \sin\left(2\pi n\frac{k}{M}\right) \tag{2.18}$$

2.5.2 Recursive Discrete Fourier Transform

The RDFT was developed at first to simplify the computational complexity of DFT since then it was widely employed in frequency detection and phasor calculations.

According to [70] RDFT was one of the fastest algorithms in power system application because it is computationally efficient. RDFT can be used to find the value of V_k for a constant k.

$$V_{k-1} = \sum_{n=a-M}^{a-1} v_n \cdot e^{-j2\pi\frac{n-1\cdot k}{M}} \tag{2.19}$$

$$V_k = \sum_{n=a-M+1}^{a} v_n \cdot e^{-j2\pi\frac{n-1\cdot k}{M}} \tag{2.20}$$

Thus

$$V_k^{NOW} = V_{k-1}^{PREV} - v_1 \cdot e^{\frac{-j2\pi n}{M}} + \cdots + v_M \cdot e^{\frac{-j2\pi nk}{M}} \tag{2.21}$$

It can be simplified

$$V_k^{NOW} = V_{k-1}^{PREV} + (v_n - v_{(n-M)}) \times e^{\frac{-j2\pi nk}{M}} \tag{2.22}$$

According to the previous there are only two multiplication, an addition and a subtraction processes required when calculating a new value, which will provide a time reduction during the calculation of the DFT. Reducing computational loss means minimum lag during synchronisation, as it will be demonstrated later.

However, solving the previous equation will require to break the exponential to real and imaginary, which means it will require double the time to solve the equation.

2.5.3 STM32F4 Microcontroller

Among the many series of digital controllers, the STM32F4 is one of the powerful microcontroller that has 32bit. It is based on ARM Cortex-M4 core and it was modified by adding many peripherals to it. The modifications were able to reach the controller to 225DMIPS/608 CoreMark when executing from flash memory at 180MHz. While it requires low power consumption that reach to $89\mu A/MHz$. The controller gathers both capabilities of the MCU unit to execute instructions and DSP. Having three ADCs on-board and the ability to generate up to six PWM with five GPIO made the controller useful for power application such as power conversion and motor control [71].

Chapter 3

A New Integrated Structure Interleaved DC Converter

3.1 The Proposed Integrated Magnetic Structure

Because all high flux ferrite cores are lossy in comparison to low flux density ones, Researchers were investigating new methods to increase the voltage gain of the boost converter without relying on large duty cycle. Adding a multiplier can be one of the methods to increase the gain. An adaptable interleaved DC boost circuit is proposed as shown in Figure 3.1. The proposed topology contains additional windings that acts as a multiplier. The windings aligned at low flux core to ensure minimum iron loss.

The topology consists of two main magnetic components, two switches and diodes. L_{in} is required to provide a current continuity during the switching overlap and to keep low current ripple on the input. The full circuit diagram is presented in appendix B.

The main magnetic structure can be considered as a non-isolating transformer consisting of four windings, where each two in a branch construct an interleaved boost converter [72]. Both branches feed through the centre point, which is connected to the input.

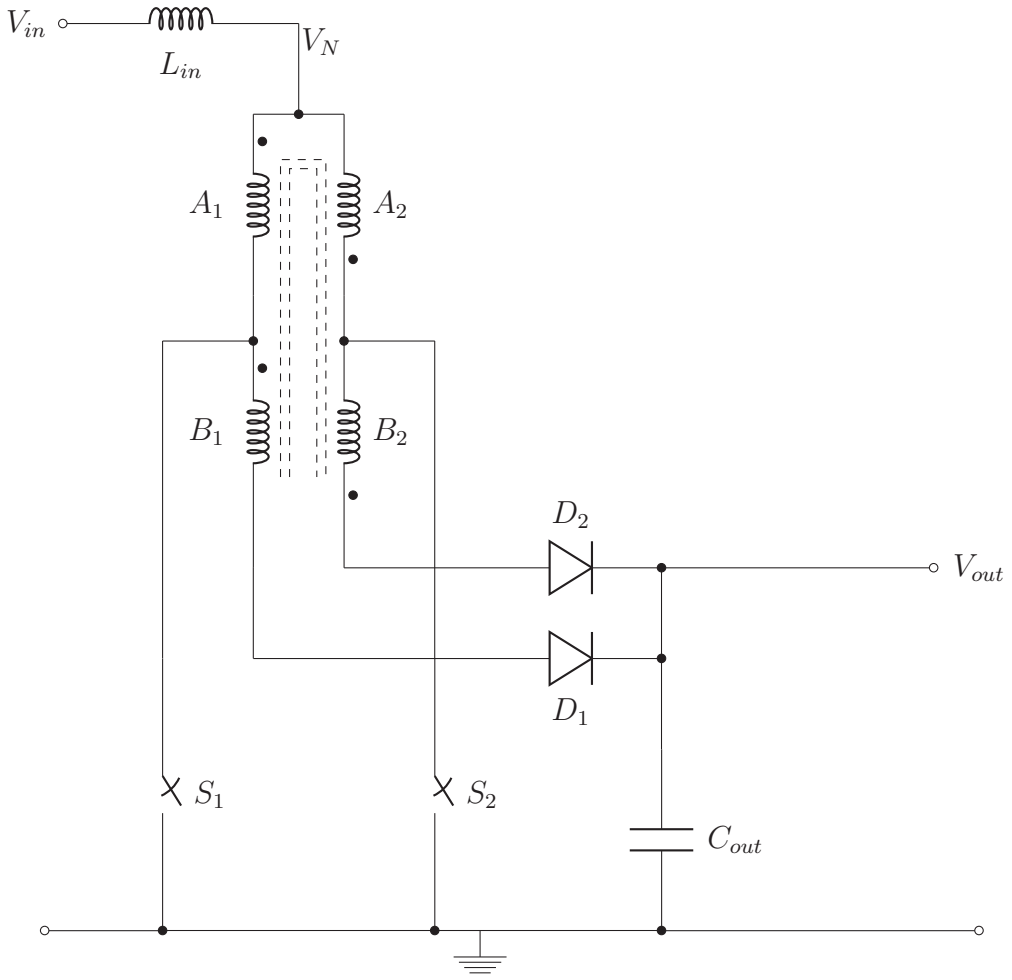


Figure 3.1: Adaptable Interleaved Boost Topology

The proposed converter has a specific switching sequence that contains an overlap as shown in figure 3.2.

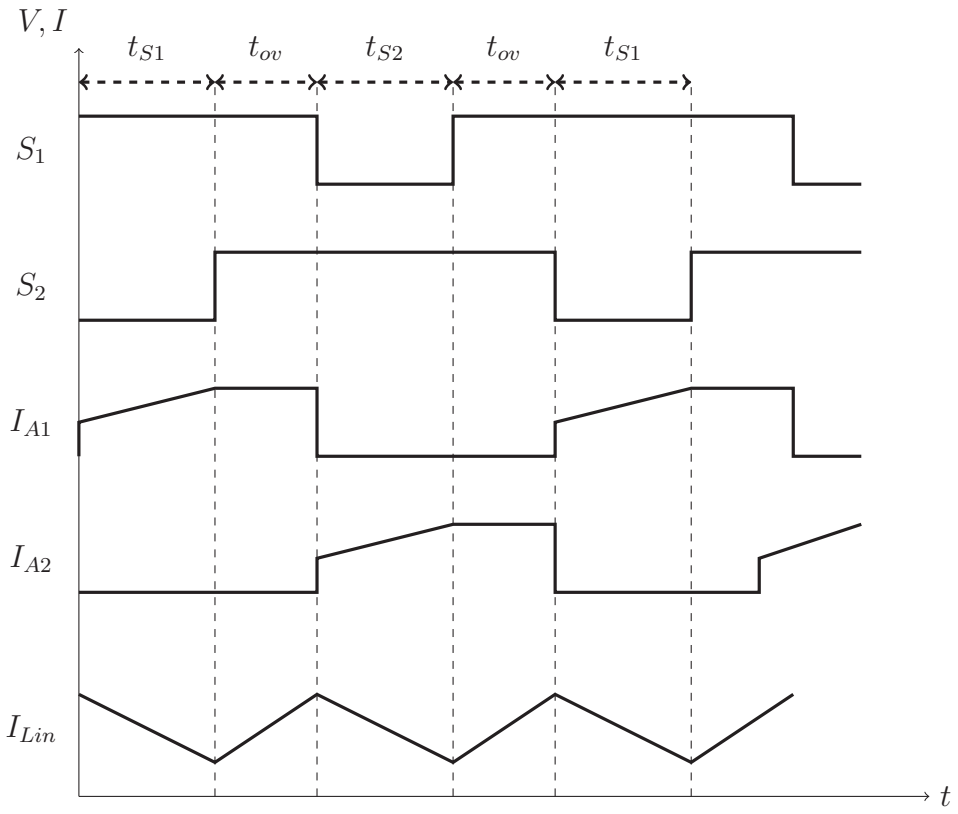


Figure 3.2: Switching Sequence and current applied to the transformer

3.1.1 Circuit Description

When one switch is closed

When one switch S_1 is closed during t_s1as shown in figure 3.2, current will flow from a central tap VN to ground through A_1 and S_1 as demonstrated in red arrows figure 3.3. The current flow will cause a potential difference ,shown in blue arrow, across the A_1 windings. Because A_1 and A_2 are magnetically coupled and their windings in the same direction, similar voltage will be presented across A_2. Likewise, the potential difference will produce across B_2 windings. While the input current I_{Lin} will fall gradually as shown in figure 3.2.

From the previous, voltage stress on the second switch S_2 will be double the input voltage imposes. While stress across $D2$ is the sum of voltages between the ground point of the switch S_1 and the anode of D_2 which are $V_{A_1}, V_{A_2}, V_{B_2}$.

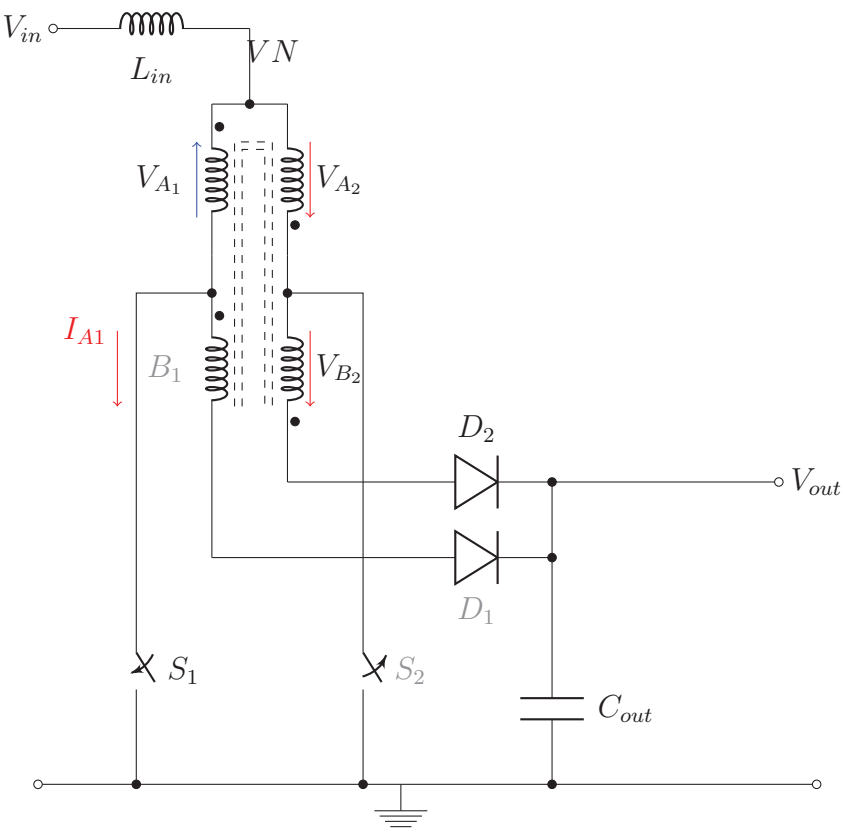


Figure 3.3: When One Switch is Closed

During this period of time D_1 will be in reverse bias and same output voltage will be applied across its terminal. This mode of operation will increase the stress across S_2 to become double the input voltage at point V_N, as shown in figure 3.13.

When Both Switches are Closed

When both switches are closed during the overlap period t_ov shown in figure 3.2, S_1 is on from the previous state and S_2 is switched ON. Theoretically, same amount of current ,shown in red in figure 3.4,will pass through the winding A_1 and A_2 as long they have the same number of turns. The current

flow will lead to produce the same value of flux around both windings. Because the produced flux from A_1 and A_2 are opposing each other, the point V_N will be virtually grounded. Grounding the centre tap of the transformer will increase the input current I_Lin leading to energise the input inductor. The amount of current incrementing through the input inductor will depend on the time when both switches are closed.

Furthermore, de-energising the transformer core will reduce the induced EMF during the turning off process of the switch, which will make no snubber circuit is required though it is subject to leakage inductance.

During this time period, both output diodes are in reverse bias and no current is fed to the output.

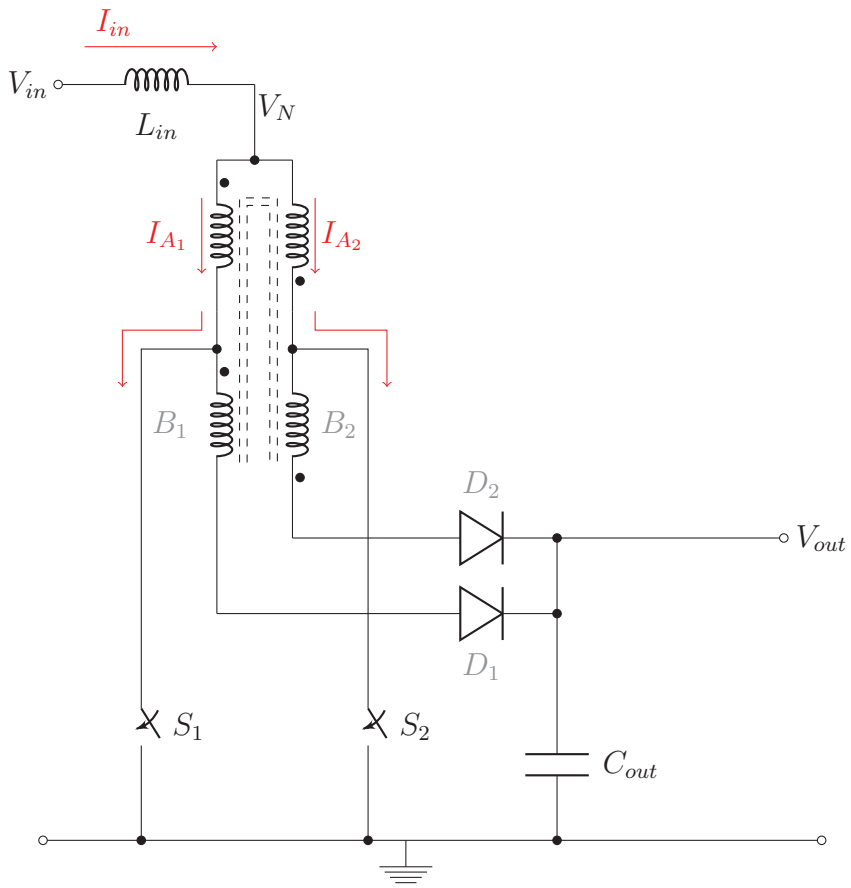


Figure 3.4: When Both Switches are Closed

The switching process of this circuit by alternation the switches with overlap will continuously change the input inductor current value. This change in the input current will cause a voltage difference across L_{in}, according to $V_L = L\frac{di}{dt}$, leading to act as a boost converter. While, the difference in turns ratio between the primary A and the secondary B windings will add extra gain by a factor of η.

3.1.2 Converter Transfer Function

To find the transfer function of the converter, two states of operation must be considered [73].

When Both Switches are Closed

The time period for this state is DT, where in this state the current is passing through L_{in} to supply both windings A_1 and A_2. Because A_1 and A_2 have the same number of turns and opposing each other then the average flux excited in the core is zero.

$$\phi_{total} = \phi_{A1} + (-\phi_{A2}) = 0$$

This will bring the centre tap point of the transformer in figure 3.1 to be $V_N = 0$ which will make it act as virtual ground, which will increase the current in L_{in} according to the equation

$$V_{in} = V_{L_{in}} = L_{in}\frac{di_{in}}{dt}$$

By assuming the incrementing is linear then

$$V_{in} = V_{L_{in}} = L_{in}\frac{\Delta i_{in}}{D \cdot T}$$

$$\Delta i_{in} = \frac{V_{L_{in}} D \cdot T}{L_{in}} \tag{3.1}$$

When One Switch is Closed

During this state that has a time period of $(1 - D)T$, the current is supplied from the source and follow through L_{in} and A_1 windings to S_1. Passing the current through A_1 windings will excite flux in the core and because A_2 and

B_2 are on the same core, an induced EMF is generated across both winding. The total output voltage of the combination can be found by summing all voltages across active windings between the ground point of the switch S_1 and the output.

$$V_{out} = V_{A_1} + V_{A_2} + V_{B_2}$$

Because A_1 and A_2 have the same turn ratio and

$$\frac{N_B}{N_A} = \frac{V_B}{V_A} = \eta$$

then

$$V_{out} = (2 \times V_A) + V_{B_2}$$

$$V_{out} = V_A(2 + \eta)$$

or

$$V_A = V_N = \frac{V_{out}}{2 + \eta} \tag{3.2}$$

Where η is the transformer turns ratio

To find the voltage across $V_{L_{in}}$

$$V_{L_{in}} = L_{in}\frac{di_{in}}{dt}$$

$$V_{L_{in}} = L_{in}\frac{\Delta i_{in}}{(1 - D)T} \tag{3.3}$$

by taking into consideration that the voltage across $V_{L_{in}}$ is

$$V_{L_{in}} = V_{in} - V_N \tag{3.4}$$

by substituting 3.2 and 3.3 in 3.4 then

$$L_{in}\frac{\Delta i_{in}}{(1-D)T} = V_{in} - \frac{V_{out}}{2+\eta} \tag{3.5}$$

by substituting equation 3.1 in 3.5 then voltage gain of the proposed topology is shown 3.6

$$\frac{V_{out}}{V_{in}} = (2+\eta)\,\frac{1}{1-D} \tag{3.6}$$

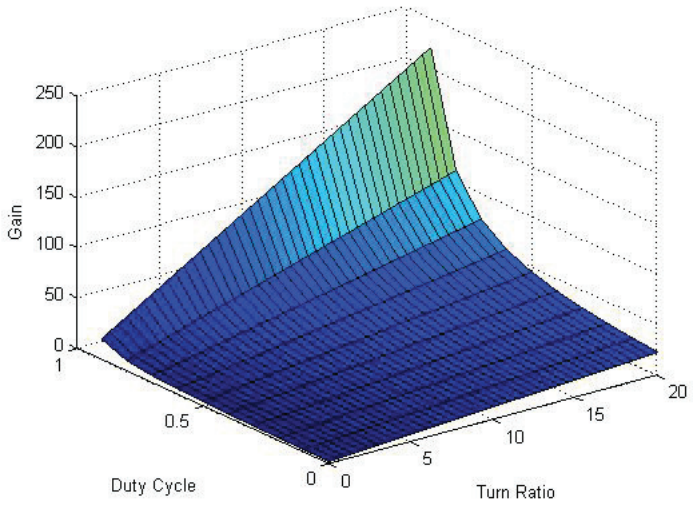


Figure 3.5: Proposed structure Gain vs Turn Ratio at Different Duty Cycle

3.2 Transformer Design

To start the procedure of designing high frequency transformer, it is required to identify the operating frequency, power rating and voltages of the system. Because the system is feeding from 200 watt PV and will supply the grid, both voltage and power can be defined.

Required Parameters	Value
Frequency	125-300 kHz
Power	200 Watt
Supply Voltage	32 $\sim$ 44 Volt
Output Voltage	310 $\sim$ 320 Volt
Input Current	10 Amp

Table 3.1: Prototype parameters

Based on the mode of operation, the magnetic structure can be considered as a non-isolation transformer rather than coupled inductor as there is no energy storage in the structure. This fact will lead to a conclusion for using high permeability materials.

Using table 3.1, finding transformer total power is initial to specify the core size later. The total power is the summation power through windings of primary and secondary.

$$P_t = P_1 + P_2$$

If the transformer efficiency is 100% then $p_t = 400$ watt.

The second step is to specify core size or area product A_pP of the transformer. Where total area product most equal or bigger than $24000mm^4$, according to equation 2.9.

The selected core of the proposed structure is Mn-Zn soft si-ferrite N87. the core EPCOS PM50 has a μ of 2200.

The selected core is capable to handle the maximum power and the wide operating frequency rated up to $1MHz$, makes it suitable for application as the flux will alternate between $125-300kHz$. The temperature is considered to kept at 43°C during the design [46]. It has a volume of $31000mm^3$, which

has area product bigger than the required one and can offer flexibility for future development. Because of PM50 is a pot type, its shape contribute to reduce leakage inductance in the transformer.

Using equation 2.7 with the help of information provided in table 3.1, the number of primary turns will be;

$$N_1 \approx 1 \; turn$$

The previous number of turns was calculated for the non-gapped core. To reduce flux density, gapping by 0.16 mm will be introduced to the core. Because gapping the core can effect on inductance value which consequently will impact the total input current, the following new number of turns is calculated to maintain the inductance ($\approx 11\mu H$) as in equation 2.3.

$$N_1 = 3 \; turns$$

for the specified air-gap a fringing factor F was calculated to ensure the accuracy of introducing choice

$$F = 1 + \left(\left(\frac{lg}{\sqrt{A_c}} \right) \times \ln \left(\frac{2 \times l_W}{lg} \right) \right) \tag{3.7}$$

Where l_W is window length and $F \approx 1$ which is acceptable for the specified design.

From table 3.1, the average gain required is 8. To improve the converter stability by making sure that the operation is in the linear part of the figure 3.5, the duty cycle should be limited between $10\% \sim 50\%$.

By taking into consideration the previous values of gain and duty cycle with help of equation 3.6, the suitable number of secondary turns are

$$N_2 = 15 \; turns$$

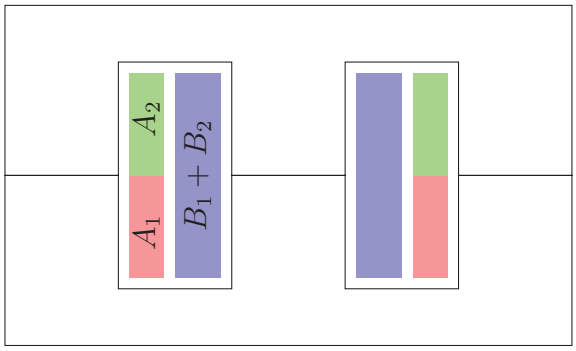


Figure 3.6: Windings Distribution in the Core

3.2.1 Flux Orientation During Operation

When switch S_1 is ON the current will flow through the A_1 windings to ground. The current will produce a flux in the core which will induce a voltage across the B_1 windings. During this operation the flux will build in one direction of the B-H curve of the magnetic core. When S_2 is ON the current will flow in the second branch through the windings A_2 to the ground, leading to induce a voltage across windings B_2.

Because the windings in both branches are opposing each other, the flowing current in S_2 will induce a flux in the negative part of the B-H curve of the core material. The current waveform with the overlap operation is shown in figure 3.2

The residual flux is minimized during the operation by introducing an overlap time. During the overlap time, both switches will be closed leading to pass the current through both low voltage windings.

The current in both branches will have a different gradient and magnitude because of the residual flux in the core. This mode will cause the voltage at the centre tap of the transformer to fall to zero (or become virtual ground), therefore L_{in} is required to provide current continuity by introducing an

impedance between the centre point and the source. Minimizing the residual flux will allow the operating frequency to increase to the core operating limit.

The magnetic structure will combine two interleaved boost converters, each consisting of a low voltage winding and a multiplier. This structure will minimize the number of magnetic components and should contribute to obtaining high efficiency for the topology where the losses are kept minimum.

3.2.2 Wire Selection and Current Density J

At high frequency, skin effect has a huge impact on the wire cross section. The effective skin depth can be found by equation 3.8 [61]

$$\delta = \frac{\Delta K_{temp}}{\sqrt{f}} \tag{3.8}$$

where $\Delta K_{temp} = 66.08$ at $20°C$ and δ is in (mm).

At the operating frequency the required diameter of the wire is 0.085mm. Taking the peak current of the primary into consideration with respect to the current density, the selected Litz wire is $7 \times 0.3mm$, while the current density is $J_1 = 3.03\ A/mm^2$.

3.3 Input Inductor L_{in}

The proposed integrated interleaved boost converter shown in figure 3.1 requires an input inductor to act as a current source and to reduce input current ripple. According to the previous, the input current waveform will be a unipolar as shown in figure 3.7 which requires a different type of materials in comparison to transformer core.

The priority for such application is to choose a material that has high DC bias capability. Alloy powder cores such as Sendust, Neu Flux, Iron Silicon (Fe-Si) and Koll Mu are suitable for storing energy.

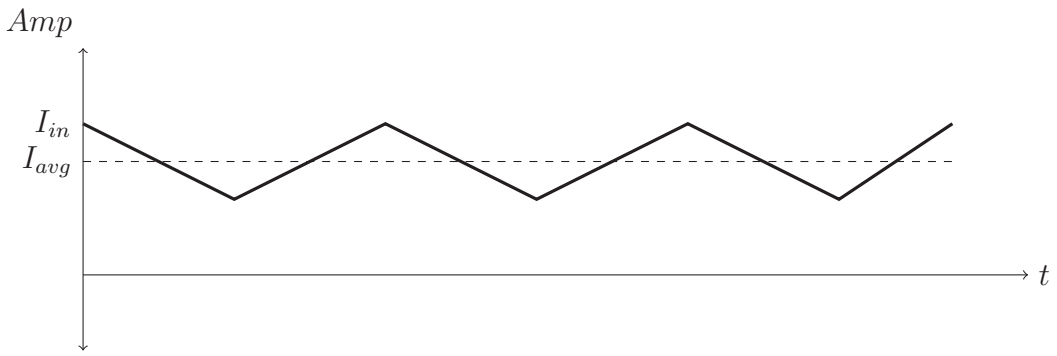


Figure 3.7: Flux Waveform in the Transformer

An equation to find the current ripple was derived to find the suitable inductance value. During the period where only one switch is closed, as shown in Figure 3.1, the voltage difference across L_{in} is given by

$$V_{L_{in}} = -L\frac{dI_{in}}{dt}$$

and

$$V_{L_{in}} = (V_{in} - V_N)$$

while $V_N = V_A$ then the previous equations can be rewritten as

$$(V_{in} - V_A) = -L\frac{dI_{in}}{dt} \tag{3.9}$$

The output voltage is given by

$$V_{out} = 2V_A + V_B \tag{3.10}$$

while the turn ratio is

$$\frac{V_B}{V_A} = \eta$$

then the output voltage can be

$$V_{out} = V_A\,(2 + \eta)$$

Or

$$V_A = \frac{V_{out}}{2+\eta} \tag{3.11}$$

by substituting equation 3.11 into 3.9, we obtain

$$V_{L_{in}} = -\left(V_{in} - \frac{V_{out}}{2+\eta}\right) = L_{in}\frac{\Delta i_{L_{in}}}{(1-D)T}$$

Rearranging this for $\Delta i_{L_{in}}$ gives

$$\Delta i_{L_{in}} \geq \frac{-\left(V_{in} - \frac{V_{out}}{2+\eta}\right)T(1-D)}{L_{in}} \tag{3.12}$$

to find the suitable inductance value, the following equation 3.12 can be used:

Following photovoltaic system demand, limiting maximum allowable input current ripple to $\Delta i_{in} = 1A$ will require $L \geq 50\mu H$

A Sendust material toroidal core MS-106125-2 was selected with dimensions of Outside Diameter (OD): 26.92mm, Inside Diameter (ID): 14.73mm, Height (Ht): 11.18mm and has an initial Permeability of 100

The required number of turns to achieve the target inductance value were 12 turns.

3.4 A New Proposed Method to Find Iron Losses

Because the losses are linked to the frequency and flux density, the classic way of calculating the core iron losses [24] will be accurate when a single tone current produces a flux. Research has been published to analyse the magnetic losses. However, this research considered the operating frequency as a pure sinusoidal waveform [74], [75], while Mn-Zn cores are usually used with switching power supplies which produce asymmetrical waveforms which contain harmonics.

In power electronics converters most of the magnetic materials are supplied with square or triangular current waveforms with variable duty cycle. This will excite a flux in the core at different frequencies [76].

$$B(t) = B_{dc} + \sum_{n=1}^{\infty} Bm_n \cdot sin(w_n t) \tag{3.13}$$

Where n is an odd integer

Because the current waveform as shown in figure 3.2 has an approximate square shape and the flux density is chosen to have a small value, the produced flux in the transformer core will have the same shape. The expected flux waveform shown in figure 3.8 is a quasi square wave with variable off time.

$$B(avg) = \frac{1}{\pi\ A_c} \left(\int_0^{\pi-\alpha} \phi_m\ dt \right) \tag{3.14}$$

By finding the odd harmonics in the waveform, we will have:

$$B(\omega) = \frac{1}{\pi_m\ A_c} \left(\int_0^{\pi-\alpha} \phi.sin(n \cdot \omega t) dt \right) \tag{3.15}$$

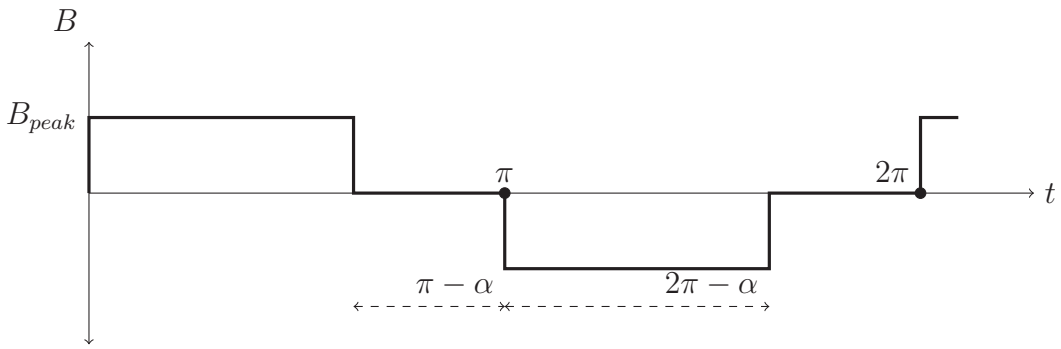


Figure 3.8: Flux Waveform in the Transformer

$$B(w) = \frac{\phi_m}{\pi \times A_c(nw)} \left[-\cos(nwt)\right]_0^{\pi-\alpha}$$

$$B(w) = \frac{\phi_m}{\pi \times A_c \times (nw)} \left[-\cos\ n(\pi-\alpha) + \cos(0)\right]$$

where

$$\cos(0) = 1$$

$$B(w) = \frac{B_{peak}}{\pi \times (nw)} \left[1 - \cos\ n(\pi-\alpha)\right]$$

The flux in the core has two components, imaginary and real, both of which will vary with respect to the field frequency. Because eddy current loss is caused only by the real component of the flux, it can be calculated thus

$$B(n) = \sum_{n=1,3,5}^{Q} \left(\frac{B_{peak}}{\pi\ (nw)} \left(1 - cos\ n(\pi-\alpha)\right) \right) \tag{3.16}$$

Where Q is the factor that is limited by the material highest operating frequency.

By substituting equation 3.16 in 2.10 and assuming the material MnZn resistivity, ρ, is constant from n=1 to Q, the effect of all harmonics and duty cycle changing on eddy current loss will be:

$$P_e(n) = K_e \sum_{n=1,3,5}^{Q} f_n^2 \cdot \left(\frac{B_{peak}}{\pi\ (nw)} (1 - cos((\pi - \alpha)n)) \right)^2 \frac{A_c}{\rho} \tag{3.17}$$

Consonantly the hysteresis loss can be found by

$$P_e(n) = K_e \sum_{n=1,3,5}^{Q} f_n^x \cdot \left(\frac{B_{peak}}{\pi\ (nw)} (1 - cos((\pi - \alpha)n)) \right)^y \frac{A_c}{\rho} \tag{3.18}$$

Where $x = 1.64$ and $y = 2.68$ as they were selected depending on the operating temperature.

In both 3.17 and 3.18, total power loss will be affected by the change of duty cycle α and the harmonic order. The equations did not take into consideration the effect of the continuous changing in material temperature during operation as it can be related to future work.

3.4.1 Windings Resistive Losses

Dealing with high power at low voltage the resistive losses can be very high due to the current value. Even the current waveform has its impact on the total wire losses when the value does not have a constant DC level. Distorted waveform can be simplified using Fourier to harmonics component [77].

Each frequency component produces a certain amount of flux around the wire that is linked proportional to its current value. Leading to have a huge amount of flux that is induced by different current components.

Each component causes a unique skin depth δ related to the its frequency as $\delta = \frac{66.08}{\sqrt{f}}$

The total winding losses can be calculated by taking into consideration all the current components as shown

$$P_{los} = I_{DC}^2 \cdot R_{DC} + \sum_{n=1}^{\infty} (I_n)^2 \cdot F_r(\omega_n) \cdot R_{DC} \tag{3.19}$$

Where I_n is the rms current value of the Fourier component at (ω_n), resistance factor F_r is the ratio of AC to DC wire resistance at a certain frequency, to find the resistance factor at different frequencies

$$F_r(\omega_n) = 1 + (F_r(\omega_1) - 1)\frac{\omega_n^2}{\omega_1^2}$$

Equation 3.19 can be employed to find the wire losses in L_{in} where the current waveform is distorted, nevertheless it can be used to find the copper loss in the transformer.

During the design, proximate effect was not considered due to having single layer of turns at the primary side. Likewise, the secondary was made of a single layer of turns. Having a one layer of turns for each will cause proximity resistance but it will not be significant.

3.5 Results on Integrated Magnetic Structure and Iron Losses Calculation

Transformer was designed and tests were carried out to verify its performance. Figure 3.9 shows the primary side inductance value of the transformer at different DC bias. This test proves the design accuracy when an effect of DC component that may produce during frequency changing. It likewise verifies the selection of core material and size. According to figure 3.9 a test of DC bias effect on the inductance. It shows that primary winding inductance changed by $0.2\mu H$ when the core biased using 6 Amp DC through the primary windings.

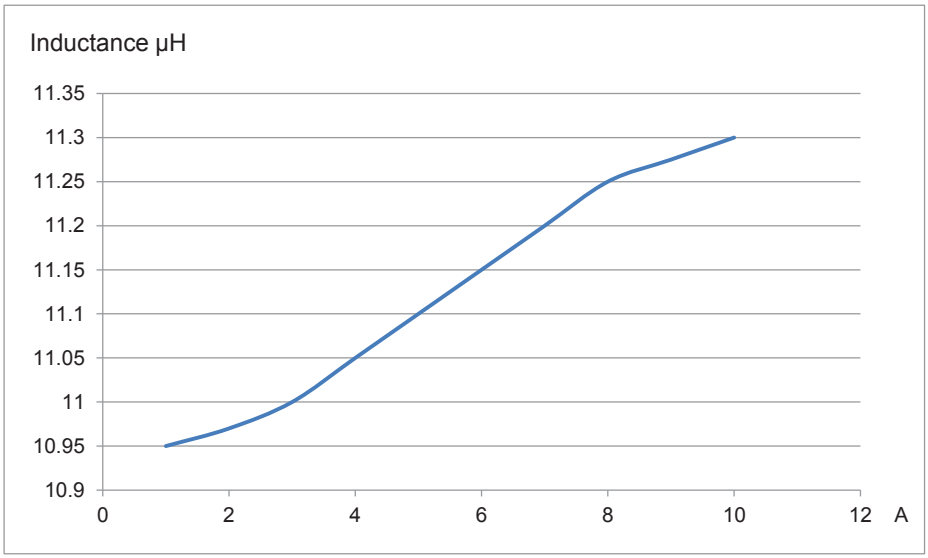


Figure 3.9: Primary Side Inductance VS DC Bias

The change in inductance value was due to the rising temperature of the core during the test and even though, it is acceptable and it verifies the selection of core size and the design concept.

The total iron loss of the core is 1.9 *watt* for a 200 *watt* system. This will provide an efficiency of 99%. According to the figure 3.10, it can be seen that the area under the curve of the flux waveform has an average value of zero. Having an average of zero means, that the windings are evenly distributed in the core and there is no DC component. This will prevent flux accumulation in any direction of the B-H curve, leading to saturation.

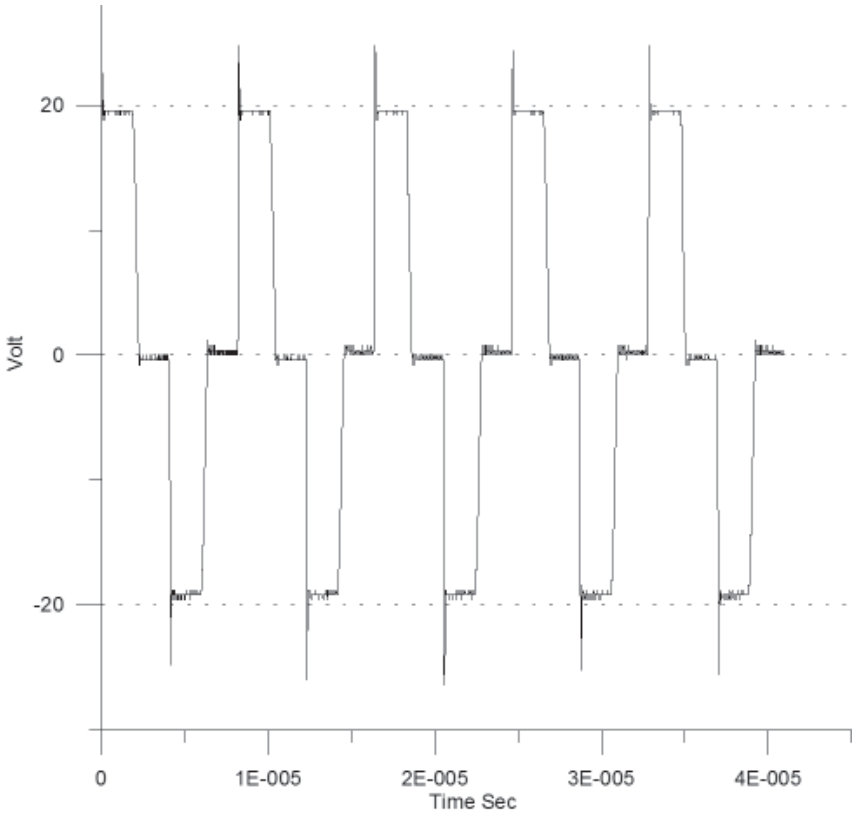


Figure 3.10: Voltage obtained from auxiliary to show the flux waveform in the core

Figure 3.10 shows the flux waveform as voltage obtained across $10k\Omega$ resister fed from half turn auxiliary winding. The waveform has a peak voltage of $20V$ and frequency of $\approx$ 130 kHz, where the low operating frequency is

used to test the circuit.

The quasi square shape of the flux waveform indicates that there are harmonics component in the flux. The magnitude of the harmonics component can vary by changing the off time of the flux waveform and it will be considered during losses calculation.

Moreover, having zero volt during the overlap time in the flux waveform, means the primary windings on both sides are having the same number of turns and the windings are equally balanced.

Figure 3.11 shows the current waveform of the A primary windings which will look same as input inductor current waveform when both waveforms added to each other as shown in figure 3.12.

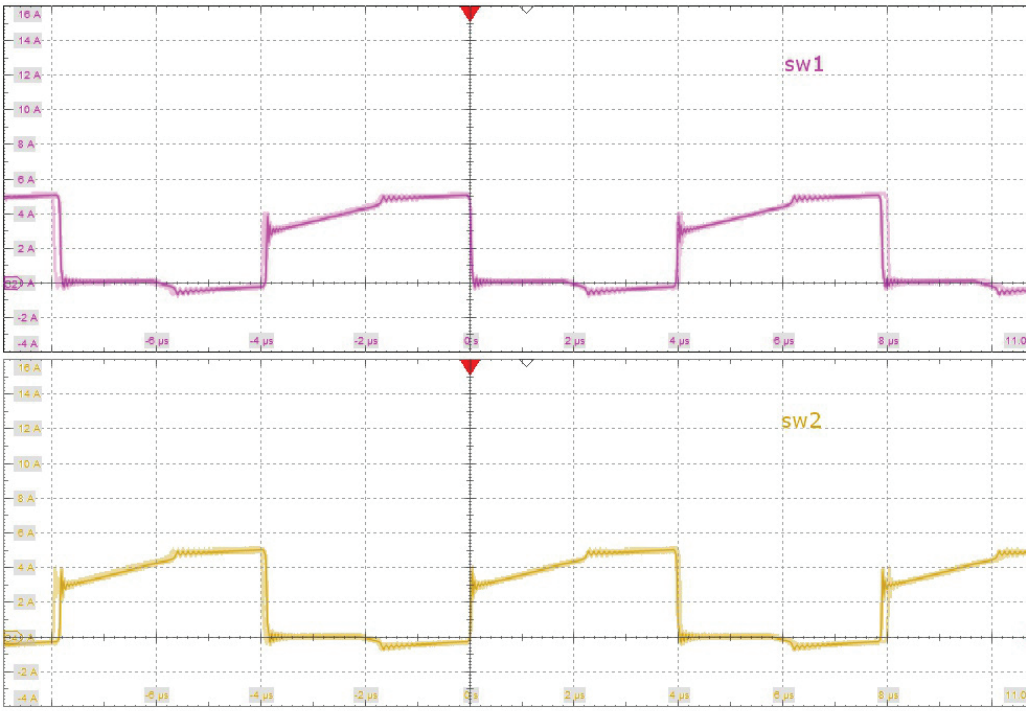


Figure 3.11: Current Waveform of the A Windings

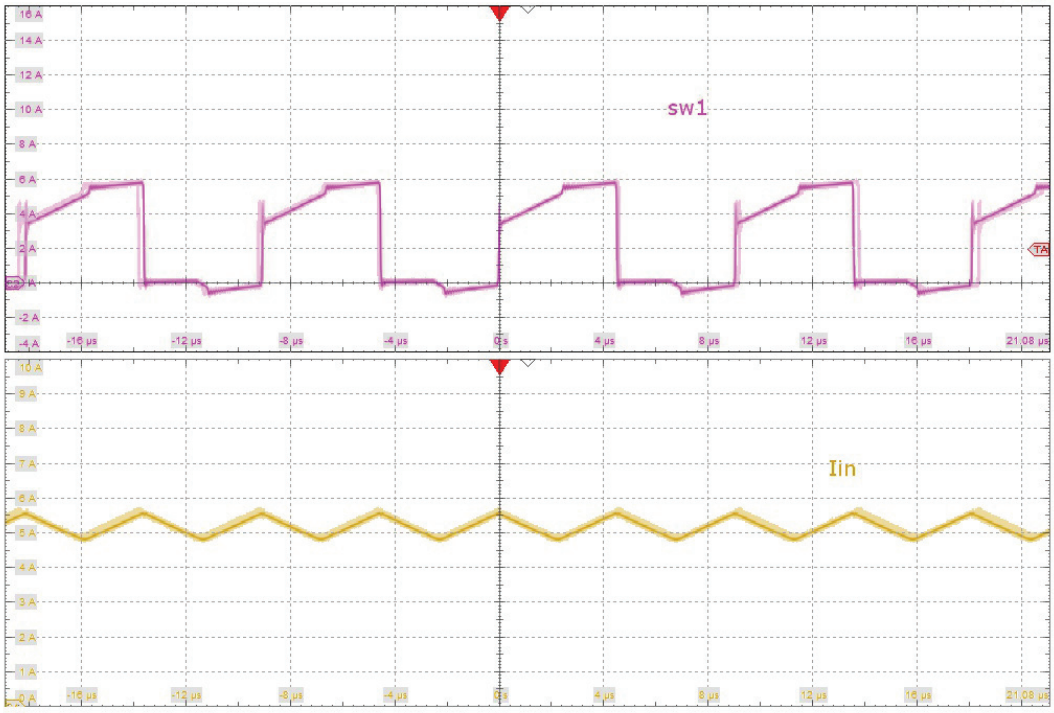


Figure 3.12: Current Waveform of the Input Inductor

Figure 3.12 shows that the rate of change of input inductor current is twice the rate of change of transformer primary current, which indicates less switching losses and smaller input inductor required. furthermore, the current ripple is limited to less than 1 *Amp* which verifies the selected value of the input inductor.

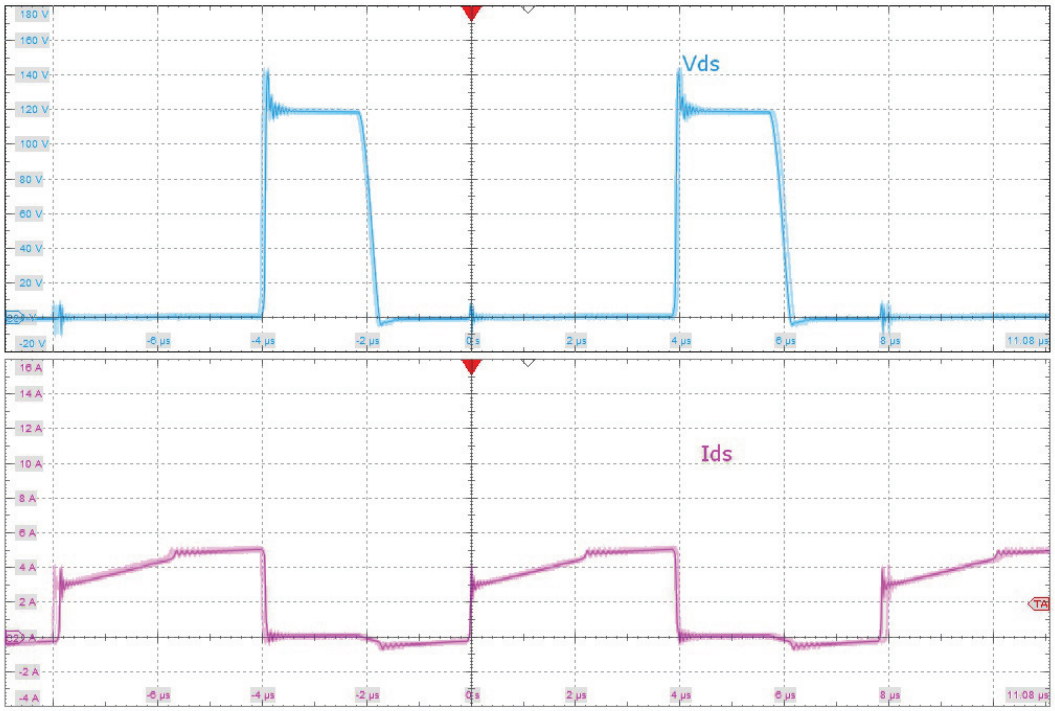


Figure 3.13: Drain to Source Voltage and Drain Current

From figure 3.13 the peak voltage across the MOSFET is the product of double the input voltage times η, which is identical to the mathematical findings. Furthermore, the figure shows that the V_{ds} has ringing when the MOSFET is off, which is due to leakage inductance of the circuit.

At the output side, the converter was capable of delivering $2A$ at $320V$ system as shown in figure 3.14. During switching the reverse voltage across output diodes was $500V$, this voltage is the reason for high reverse conduction losses.

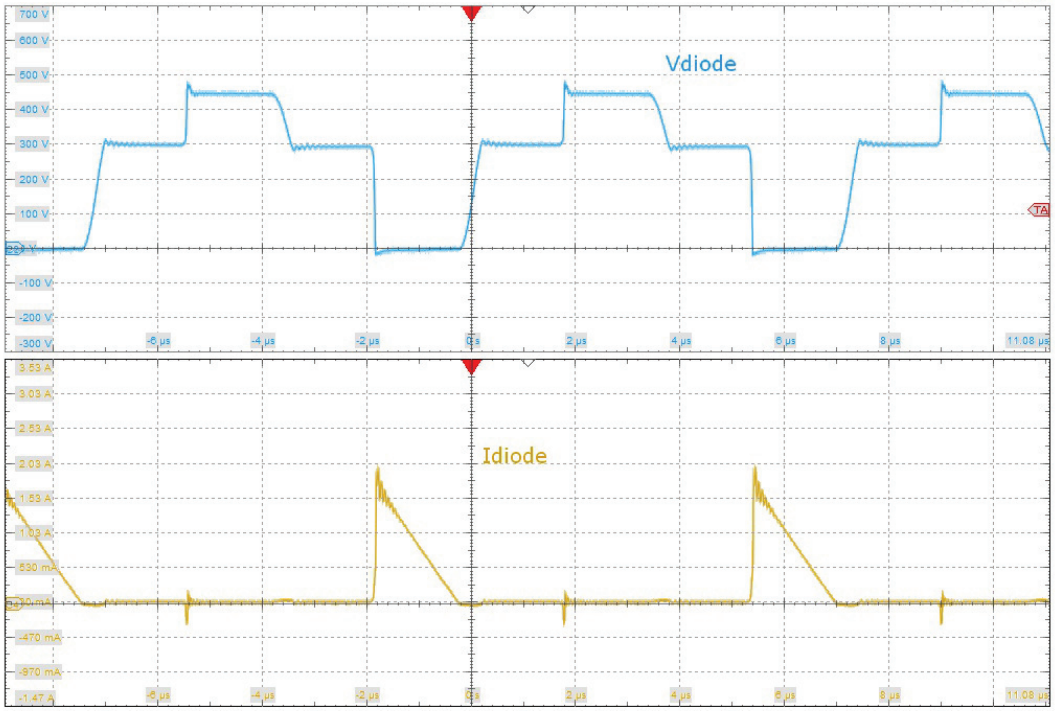


Figure 3.14: Output Diode Voltage and Current

It can be noticed from the previous figure 3.14, the converter is operating in Discontinuous Current Conduction mode (DCCM). The DCCM is suitable mode to operate all boost type converters.In order to match the impedance at both sides of the converter, variable frequency control was use with fixed duty cycle. Where the duty cycle was pre-set to a value that is in the linear region of figure 3.5. There is another factor to determine the duty cycle, this factor can affect the total loss as it will demonstrate later.

The design priority was to have a flux density of $0.015T$ in order to reduce the iron losses. Using MATLAB software, figures 3.15 and 3.16 were produced to show the optimum number of turns and the operating frequency for the $0.16mm$ gapped core.

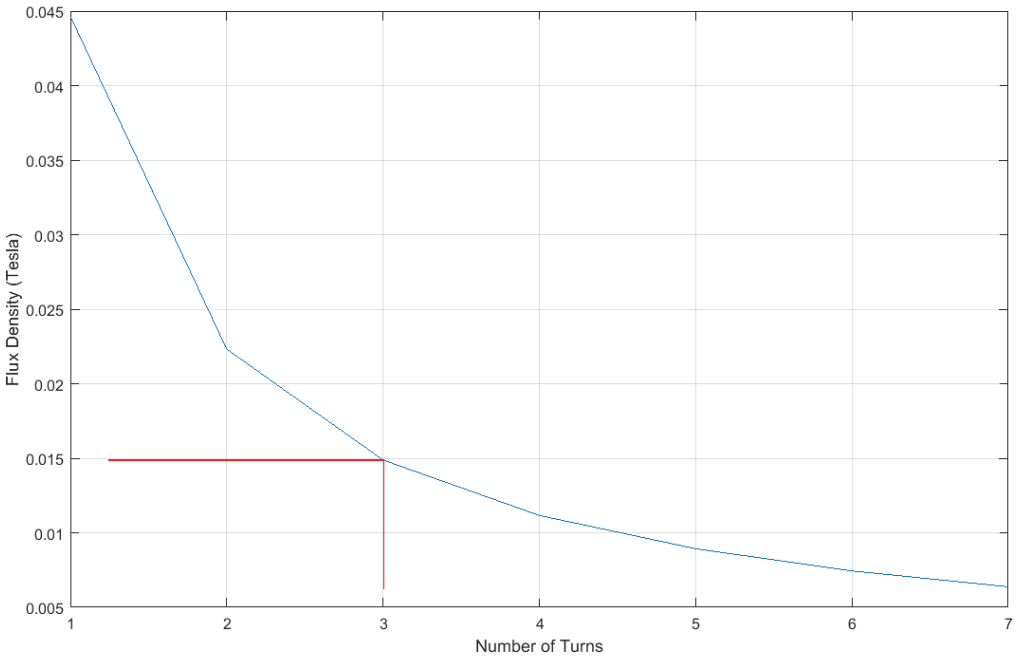


Figure 3.15: Flux Density at Different Number of Turns

By referring to the previous figure 3.15 it can be seen that three turns can be used to obtain 0.015 Tesla.

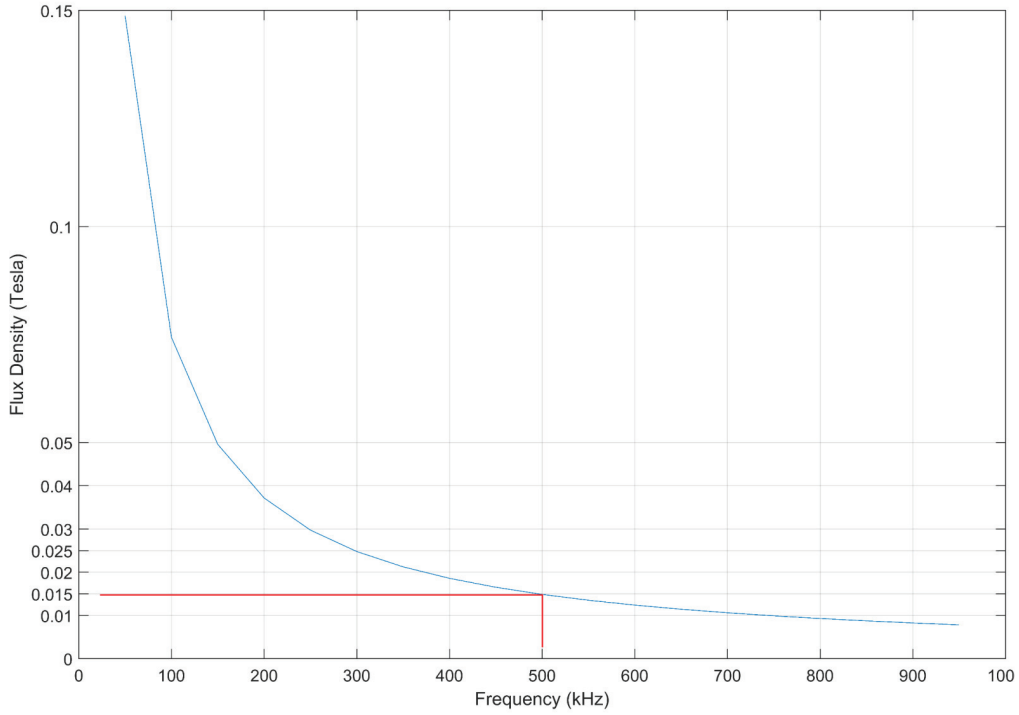


Figure 3.16: Flux Density at Different Frequencies

According to figure 3.16, the flux density value can vary between 0.015 to 0.025 Tesla depending on the operating frequency. However, changing the flux density will affect the transformer losses. Likewise, it will leave an impact on the switching devices stresses due to the change in the current value

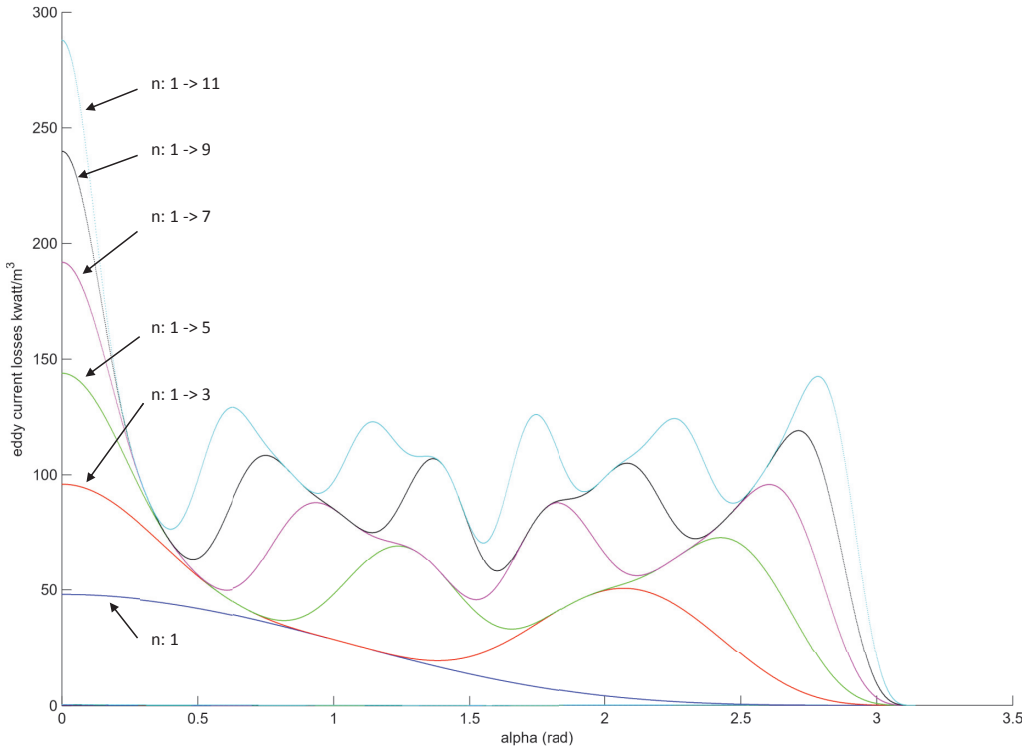


Figure 3.17: Eddy Current Loss VS α with respect to Different number of harmonics

Figure 3.17 was plotted for core PM50 that is made of N87 and operating at $200kHz$, it shows the expected eddy current loss per unit volume according to the proposed method. The quasi square waveform of flux is analysed at different α where $\alpha = (2\pi - Duty\ Cycle)$. The magnitude of flux waveform *sinc* was changing depending on α value. The eddy current loss was calculated according to harmonics contents at each α and added to the main loss of the fundamental component. It is clear the total loss increased by significantly at $\alpha = 0$, while it increases by 300% at $\alpha = \frac{\pi}{2}$.

By considering the operating frequency of the converter is $200kHz$ and the core highest rating of operating frequency is $1MHz$, then the 5^{th} harmonic

is the highest frequency that the core can respond to. Using figure 3.17, the trace labelled $n = 1 \rightarrow 5$ at $\alpha = 0.30° = 0.523\ rad$ shows the eddy current loss is 55 kW/m^3, which is approximately $1.705 Watt$. Where the eddy current loss, shows an increment of 20% in comparison to the classical method. The new calculated losses value is identical to the practical results.

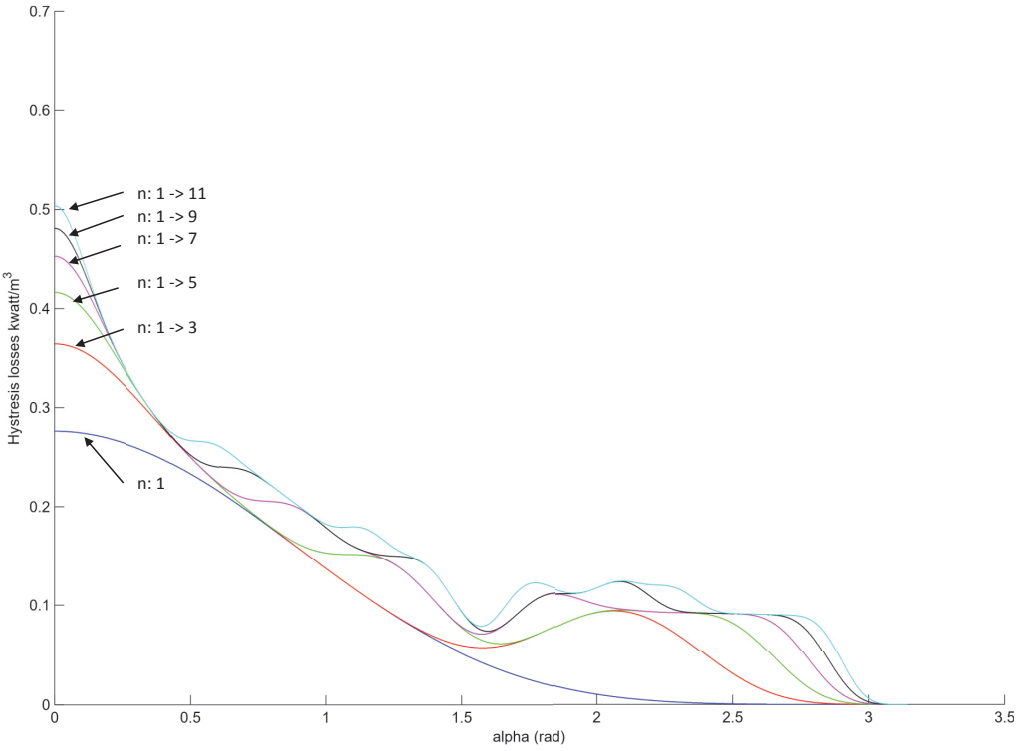


Figure 3.18: Hysteresis Current Loss VS α with respect to Different number of harmonics

Changing α will likewise affect the Hysteresis loss due to the change in total harmonics component. Figure 3.18 shows the effect of the harmonics components on the loss, where the total hysteresis loss increased by 22%. However, the loss for $\alpha > 0$ is not significant.

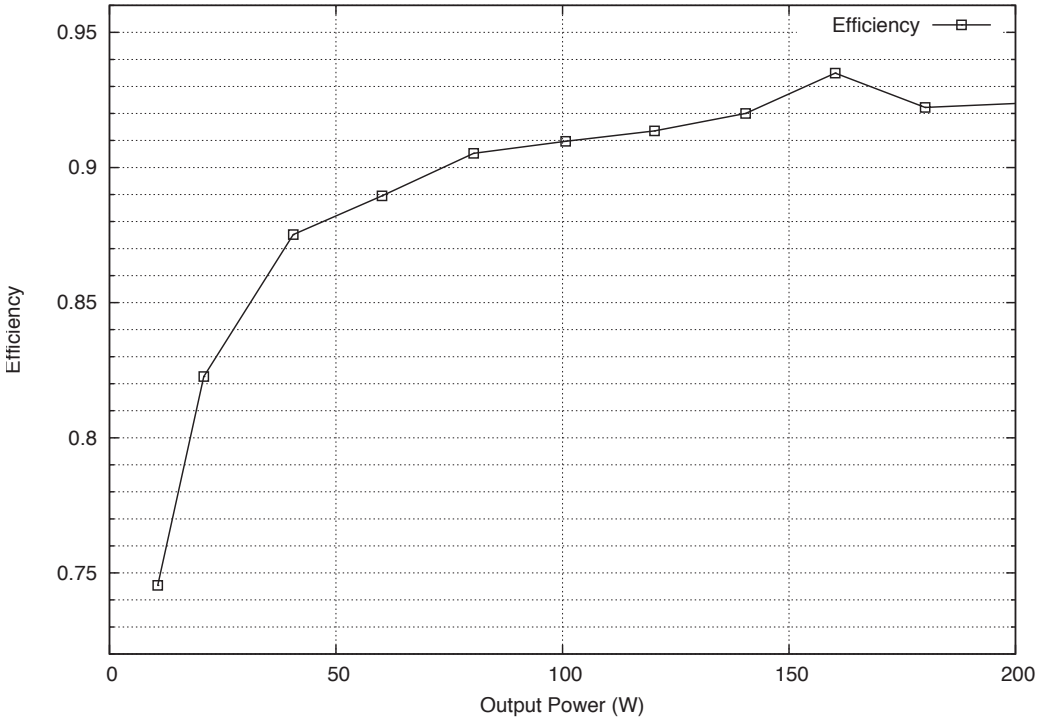


Figure 3.19: The proposed converter efficiency

From the prototype practical test, the converter efficiency reached 93% as shown in figure 3.19, this value is subject to increase depending on the quality of the components. The transformer iron losses where $2W$, which should make the converter 99% efficient. Using the new proposed method to find the losses, it can be noticed that both practical and mathematical losses calculations where identical.

3.6 Comparing Performance to Previous Research

In order to verify the usability of the proposed converter, a comparison is made to demonstrate the advantages of the converter.

Topology	Gain	MOSFET Stress	Diode Stress	Duty Cycle
Tapped Inductor Boost	$\frac{1+(N\times D)}{1-D}$	$\frac{V_{in}}{1-D}$	V_O	$0 \leq D \leq 1$
Interleaved Boost	$\frac{1+D}{1-D}$	$2 \times V_{in}$	V_O	$0 \leq D < 0.5$
Boost Converter	$\frac{1}{1-D}$	$\frac{V_{in}}{1-D}$	V_O	$0 \leq D \leq 1$
Full-Bridge	N	V_{in}	$V_{in} \times N$	$0 \leq D < 0.5$
The Proposed Converter	$\frac{2+\eta}{1-D}$	$2 \times V_{in}$	$\frac{(2+\eta)V_{in}}{1-D} + V_O$	$0.5 \leq D < 1$

Table 3.2: Comparison of Different Boosting Strategy

It is clear from table 3.2 that all the types of boost converter are relying on changing the duty cycle to obtain a specific gain excluding the full-bridge converter that its gain is limited by the number of turns of the transformer. Likewise, the proposed converter can offer the highest gain ratio, where $2+\eta$ is the factor that distinct this converter from other boost types. Galvanic isolation can be provided by the full-bridge, unlike other types of boost. Though, this mainly depends on the PV connection topology as it can be provided at the inverter side.

Having high voltage stress on semiconductors can cause a huge amount of losses while switching. From table 3.2 the proposed converter has double the input voltage shown across the MOSFETs during switching, however the converter switches are required to operate at half the converter frequency due to the overlap, which can improve the efficiency. Where having two switch

with the overlap period led to reduce switching loss to half. Unfortunately, voltage stress on diodes are the highest among the list, which can leave an impact on efficiency.

Chapter 4

A New Synchronisation Method for Grid Tie Inverters

4.1 The Proposed Synchronisation Method

With the improvement of micro-controllers, digitizing power systems has become a need to use the benefits of modern controllers. For grid tie inverters, measuring the periodic signal to obtain waveform parameters using a digital system requires transforming the measured data to a vector using DFT. During vector measurement, there are three factors, which are the rotation speed, the magnitude and the phase angle should be found during. Ideally, grid waveform is continuously oscillating around 50 Hz, the proposed algorithm in this research is suggesting a method to measure the actual frequency [78].

Because grid frequency can vary within a certain limit, usually between 48Hz and 52Hz. The suggested algorithm will use the variation limits of the grid frequency to employ the DFT with fixed window width that is tuned to both mentioned frequencies.

The First step is to transfer the waveform to a digital system by sampling the input signal, the number of samples must be a positive integer that is multiple of the measured frequency, according to the following.

$$f_(measured) = \frac{k \cdot f_s}{N} \tag{4.1}$$

where f_s is the switching frequency.

Because employing DFT will require hough computations, using shifting buffer will reduce the time required. This mathematical method of reducing the execution time of DFT is known as RDFT. The RDFT tool will generate real and imaginary numbers that will vary according to the input. The output of the RDFT will follow the property of *sinc* function at both bins. Because the research focuses on using two RDFT method to measure grid frequency, both values are chosen between the operating limits of the grid frequency variation. Practically the selected frequency which have a magnitude of Hb and Ha as in figure 4.1.

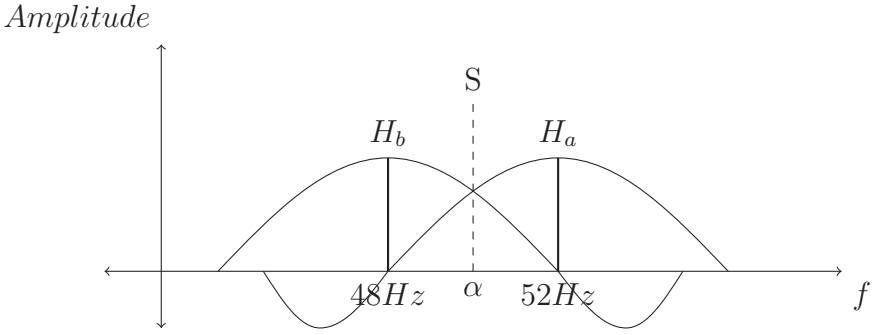


Figure 4.1: Two Frequency Points Measurement with Difference of 4Hz

If the grid waveform operates at exactly 50 Hz, both of Hb and Ha will have the same value and by drawing the envelope of *sinc* function for the two RDFT, both envelopes should interact at α point.

By assuming that the grid is not operating at 50 Hz, the following equation can be used to find the magnitude and frequency at point α.

$$H_a \cdot sinc(52 - \alpha) = S \tag{4.2}$$

$$H_b \cdot sinc(52 - 4 + \alpha) = S \tag{4.3}$$

Where both Ha, Hb are unity and represent the magnitude of the measured frequency point. Solving the equations 4.3 and 4.2 should have the same values and can be rewritten as

$$H_a \cdot \frac{sin(52 - \alpha)}{52 - \alpha} = S \tag{4.4}$$

$$Hb \cdot \frac{sin(48 + \alpha)}{48 + \alpha} = S \tag{4.5}$$

Applying Taylor series can be one of the methods to solve the equation to find α as follows

$$sin(52 - \alpha) = (52 - \alpha) - \frac{(52 - \alpha)^3}{3!} + \frac{(52 - \alpha)^5}{5!} - \frac{(52 - \alpha)^7}{7!} + ... \tag{4.6}$$

or it can be rewritten as

$$sin(52 - \alpha) = \sum_{i=0}^{\infty} \frac{(-1)^i}{(2i + 1)!}(52 - \alpha)^{2i+1} \tag{4.7}$$

where i is an integer value.

As it can be seen solving the *sinc* function can lead to a series of sequential mathematical equations which requires a huge time to be solved and leads to make the solution inefficient. To solve this obstacle, the research will follow linear approximation method as one of the solution to reduce the computational time.

Alternatively, assuming a linear change of the intersection point of both *sinc* functions will reduce the computational loss significantly and provide an accurate method of frequency measurement.

This method can be best described as, measuring the frequency using the RDFT magnitude. Referring to figure 4.2 This can be performed by drawing a straight line between the peak of the 52 Hz point and end at 48 HZ. This will shape a triangle that has a unity height and a base of 4 Hz.

The height of the triangle will be changed with respect to the RDFT output values. This variation will lead to move the interaction point α along the scale of $4Hz$.

Practically, when $Hb = 1$ and $Ha = 0$ then the measured frequency should be $48Hz$, while if the $Hb = 0$ and $Ha = 1$ then the measured frequency should be $52Hz$. Moreover, having the same value for both will indicate a $50Hz$.

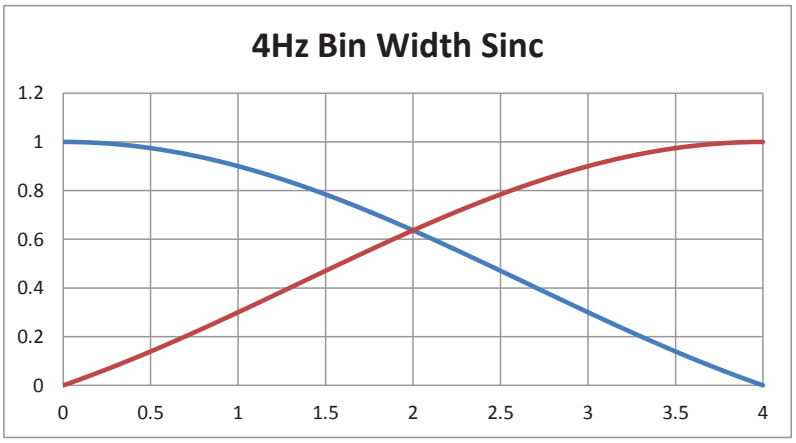


Figure 4.2: two *sinc* function interact with bin difference 4Hz

4.2 Finding Frequency Deviation

The following mathematical derivation can be used to find the frequency deviation of the input waveform by employing straight line approximation.

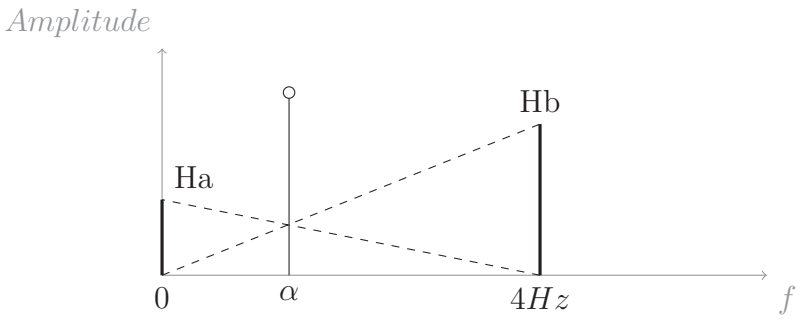


Figure 4.3: Two Frequency Points Measurement with Difference of 4Hz

$$x = 0 \Rightarrow y = Ha$$

$$y = 0 \Rightarrow x = bin\ width$$

$$ya = Ha - \frac{Ha}{bin\ width} \times x \tag{4.8}$$

$$yb = 0 + \frac{Hb}{bin\ width} \times x \tag{4.9}$$

the intersection point occurs when $ya = yb$

$$\frac{Hb}{bin\ width}x = Ha - \frac{Ha}{bin\ width}x$$
$$(Hb + Ha)\frac{x}{bin\ width} = Ha$$

then

$$x = bin\ width\frac{Ha}{Hb + Ha} \tag{4.10}$$

where in equation 4.10, x represents the frequency deviation across the $4Hz$ bin width.

4.3 Frequency Correction

With the help of linear approximation, the ratio of frequency deviation can be determined based on equation 4.10, which will help to find the actual

frequency.

$$f_{dev} = 4 \times \frac{Ha}{Hb + Ha} \tag{4.11}$$

By employing equation 4.11, the value of frequency deviation will determine by relaying on the intersecting point α of the two bins. Finding that point will not determine the actual signal frequency. Rescaled the deviation will be required to find the actual value of operating frequency, according to 4.12.

$$f_{act} = 52 - f_{dev} \tag{4.12}$$

4.4 Calculation of the Magnitude

Calculating the voltage of grid waveform is the second step following estimating the actual frequency. After applying RDFT, the grid waveform was transformed to a vector with certain length, as shown in figure 4.4, and equation 4.13 can be used to find the length.

$$Vector\ Length = \sqrt{Real^2 + Imag^2} \tag{4.13}$$

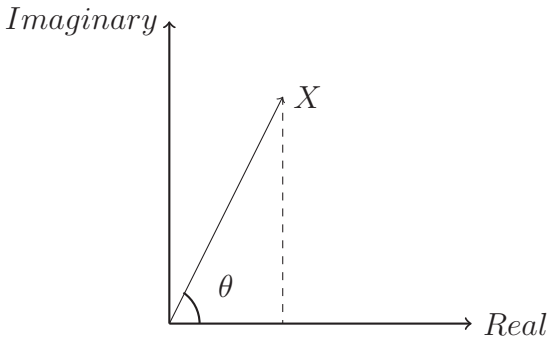


Figure 4.4: Phase Measurement

Unfortunately, the vector length will not represent the actual voltage of the grid waveform, because it forms the output of trigonometric functions, and it is required to normalised it as follow.

A lookup table of *Sinc* function was generated with respect to the calculated frequency. The *Sinc* magnitude has an amplitude of unity and width of 2Hz limit, where it can cover half the range of frequency from 50Hz to 52 Hz, while the second *Sinc* can be mirror image.

Equation 4.14 can be used to find the actual magnitude.

$$Amplitude = \frac{Vector\ Length}{StoredMagnitude} \tag{4.14}$$

4.5 Phase Measurement

To calculate the phase angle θ of the grid waveform, both real and imaginary values of RDFT outputs is used.

applying the inverse of trigonometric tangent *atan* function to both imaginary and real of DFT according to equation below will determine the Phase angle of the input signal.

$$\theta = atan\frac{Imag}{Real} \tag{4.15}$$

By applying the proposed method, there are 20 synchronisation point in one cycle where:

$$Synch\ points = \frac{f_s}{f} = \frac{1000}{50} = 20 \tag{4.16}$$

As shown in equation 4.16 the sampling process will repeat itself twenty times. Each time, it acquire 250 samples during one duration of the grid waveform. This indicates high precision to resynchronise in case of frequency drifting.

To find the spacing of phase measurement to the synchronisation points.

$$Phase\ spacing = \frac{360}{20} = 18^{\circ}$$

at 50Hz.

From the previous equation, the algorithm can resynchronise after 18° of vector rotation or there are 18° between synchronisation points. As it previously demonstrated, this value is relying on the number of samples and switching frequency.

The code was written using embedded C language with the help of Kiel compiler as it is shown in appendix D

4.6 Simulation of the Proposed method

A simulation code was written using MATLAB to demonstrate an approximate behaviour of the proposed method. The code can show how the algorithm will respond to the variation of grid frequency. Likewise, it can show the error in frequency measurement as it is tested at different frequencies. Three frequencies 51,50 and 49 Hz were selected to perform the simulation and same Fast Fourier Transform (FFT) parameters that were used in the hardware were used to ensure the performance. Where $fs = 1000Hz, N = 250, Ka = 12, kb = 13$.

A *Sinc* function was created as a subroutine, to show the simulation steps clearly, as follows.

```
function [y] = mysinc(x)
if(x == 0)
y = 1.0;
```

```
else
y = sin(pi*x)/(pi*x);
end
end
```

It is shown in figure 4.5, when the input frequency is 50Hz, both *Sinc* functions had the same magnitude and it is clear that the bins at 12 Hz and 13 Hz had the same hight.

Unfortunately, in normal situation the measured frequency does not occur on the specified bins, which can cause spectral leakage. Consonantly, the spectral leakage can generate an error that will be affected the magnitude measurement of the main bins. Such error is shown as a magnitude error of bins at 11 and 14 Hz. However, because the error had the same effect on both functions, this can eliminate the error impact during frequency calculation.

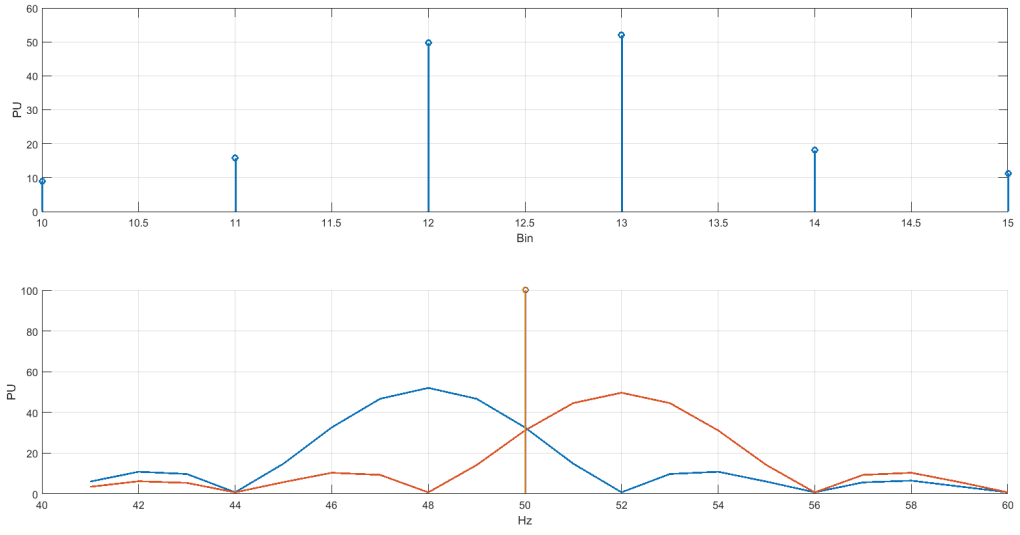


Figure 4.5: Intersect Point of Two Sinc at 50Hz

The response of the algorithm for 49Hz will be causing an increment in

the magnitude of the FFT bin at 12 Hz and reduction in the magnitude of bin at 13 Hz. On the other hand the intersection point of two *sinc* functions will be pushed further to 52 Hz and to correct that equation 4.12 is used as shown in figure 4.6. It can be seen in figure 4.6 there are two vertical lines at the intersection point, the displacement in x- axis between them is representing a computational error in frequency measurement if the tested signal is sinusoidal waveform.

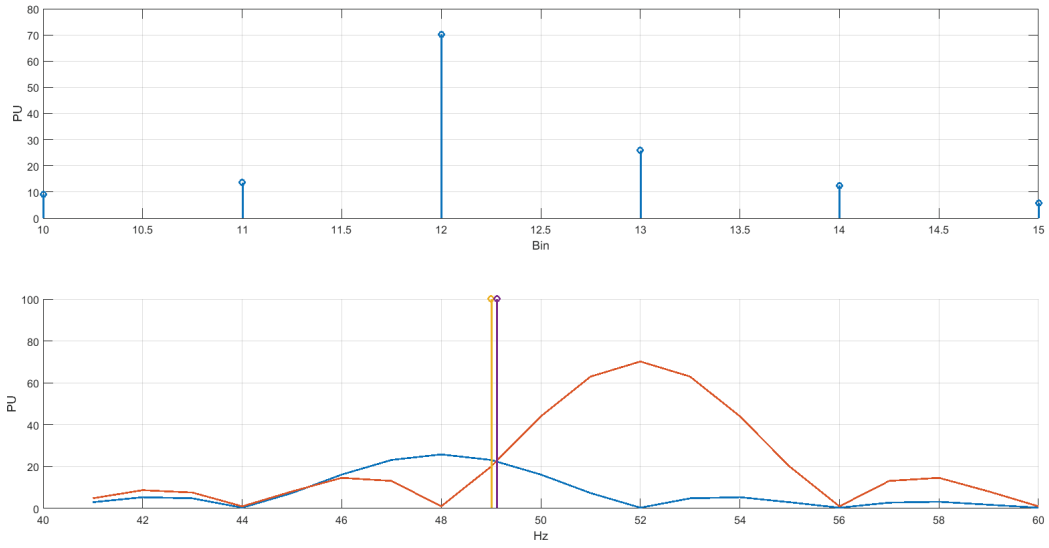


Figure 4.6: Intersect Point of Two Sinc at 49Hz

The same effect was obtained when the signal frequency is shifted to 51Hz, though this time the FFT bin at 13 has much higher value as shown in figure 4.7.

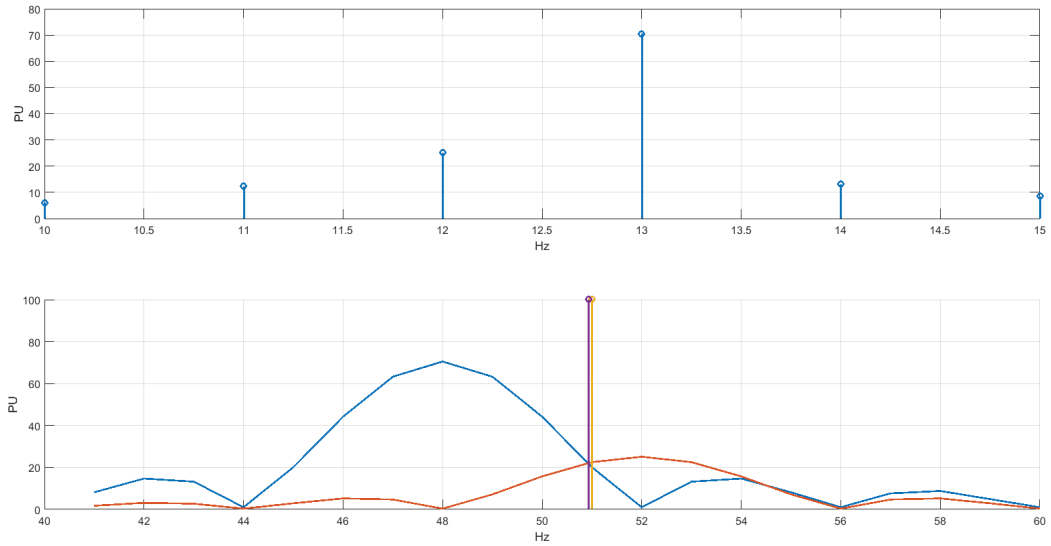


Figure 4.7: Intersect Point of Two Sinc at 51Hz

Unfortunately, if the tested waveform is distorted, then the calculated frequency using the proposed method will be slightly shifted from the fundamental. The error is due to the harmonics of the truncation waveform when DFT was used. Figure 4.8 shows the frequency measuring error when tested signal was Square wave that had a time period of 20ms and 50% duty cycle.

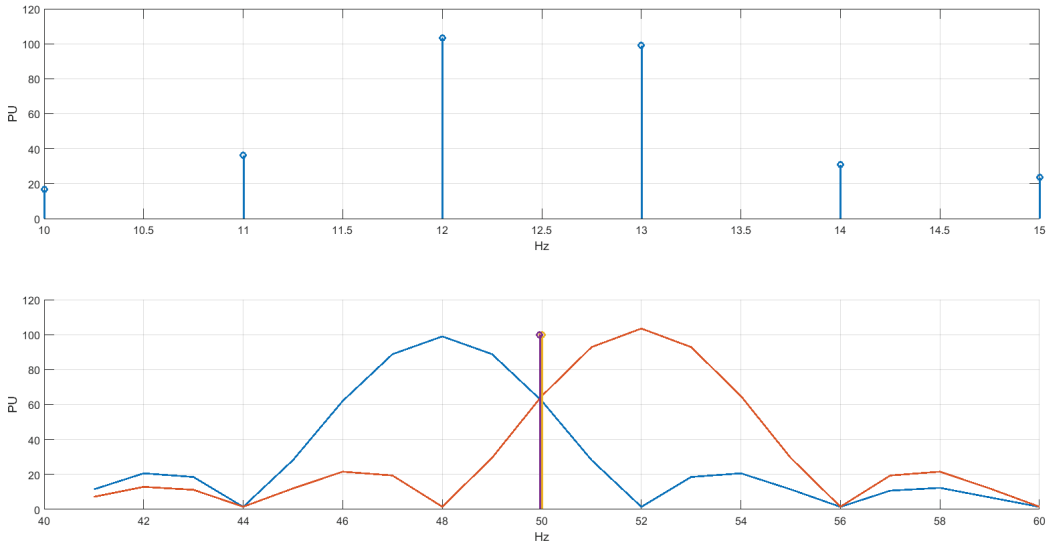


Figure 4.8: Effect of Square waveform on measuring frequency

Another factor can affect measuring frequency is the phase angle of the truncated waveform. According to the simulation program, Figure 4.9 shows the response of the algorithm between $48Hz$ to $52Hz$ at $\phi = \frac{\pi}{2}$. It can be seen that the error in magnitude is limited by $\pm 0.04035\%$. The summation result of magnitude and error can effect on measuring fundamental frequency. Though, by knowing error boundaries and correspondent phase angle, the error can be normalised as it will be suggested as future work.

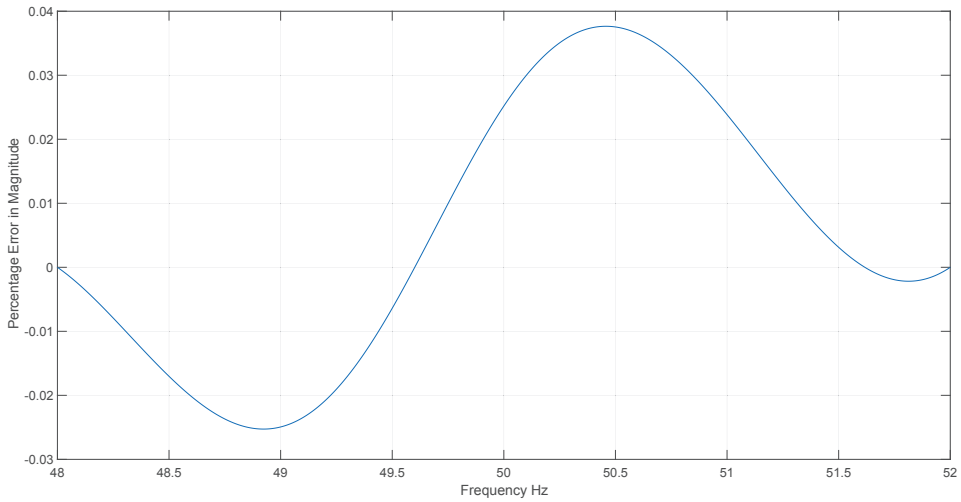


Figure 4.9: Error in Magnitude due to spectral leakage

4.7 Validity of the proposed method

To prove the validity of the straight line approximation method using two *Sinc* functions

Let assume both functions are placed by 1 per unit away from each other,

$$Ha = a\frac{sin(\pi x)}{\pi x}$$

$$Hb = b\frac{sin(\pi(1-x))}{\pi(1-x)}$$

The intersecting point occurs when $Ha = Hb$ at the mid point.

$$a\frac{sin(\pi x)}{\pi x} = b\frac{sin(\pi(1-x))}{\pi(1-x)}$$

by rearranging the previous equation

$$\frac{a}{b}\cdot\frac{\pi(1-x)}{\pi x} = \frac{sin(\pi(1-x))}{sin(\pi x)} \tag{4.17}$$

By solving the factor $sin(\pi(1-x))$

$$sin(\pi - \pi x) = cos(\pi x)sin(\pi) - cos(\pi)sin(\pi x)$$

but $cos(\pi x)sin(\pi) = 0$ then

$$sin(\pi - \pi x) = -cos(\pi)sin(\pi x)$$

$$sin(\pi - \pi x) = -(-1)sin(\pi x)$$

substituting the previous in equation 4.17, it can rewritten as

$$\frac{b}{a} \cdot \frac{\pi(1-x)}{\pi x} = \frac{sin(\pi x)}{sin\pi x}$$

$$\frac{a}{b} = \frac{(1-x)}{x}$$

Solving the previous equation will lead to

$$x = \frac{b}{a+b}$$

From the previous, result can demonstrate the validity of straight line approximation in measuring continuous signal frequency.

4.8 Hardware Requirements for the Experimental Setup

Controlling any power electronic devices using micro-controller requires great care due to voltage rating difference. Buffering and voltage level shifting are the main points that the interfacing circuit should address.

Voltage transducer An Operational Amplifier (Op-Amp) LM358 is connected as a non-inverting amplifier with DC value adjust is used as a transducer. This stage will allow to feed the grid voltage into the microcontroller with suitable voltage rating 3.3V as shown in Figure3.1.

The non-inverting amplifier gain is found by

$$G_V = V_i \frac{33k}{100k} \times \left(1 + \frac{33k}{100k}\right) \tag{4.18}$$

where the input voltage $V_i = 5 \times \sqrt{2}$

The schematic of the level shifter is shown in figure 4.10 and the prototype circuit is shown in the appendix E figure E.1

Grid waveform emulator To emulate frequency variation of grid waveform, a function generator that is able to generate distorted waveform was built. The schematic shown in 4.11 compromises a single integrated circuit ICL8038 with the ability to control duty cycle and frequency. By adjusting both $10k\Omega$ variable resisters, a distorted waveform with a range of 48 Hz to 52 Hz can be generated that is asymmetrical around y-axis. the circuit output was fed to the ST Discovery board to PA1, where the ADC is located.

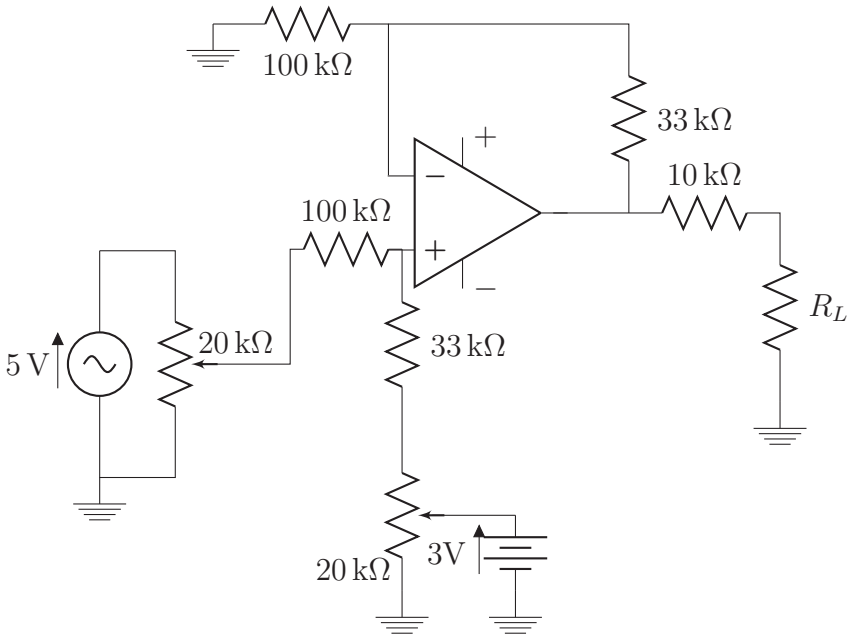


Figure 4.10: Non-Inverting Level Shifter

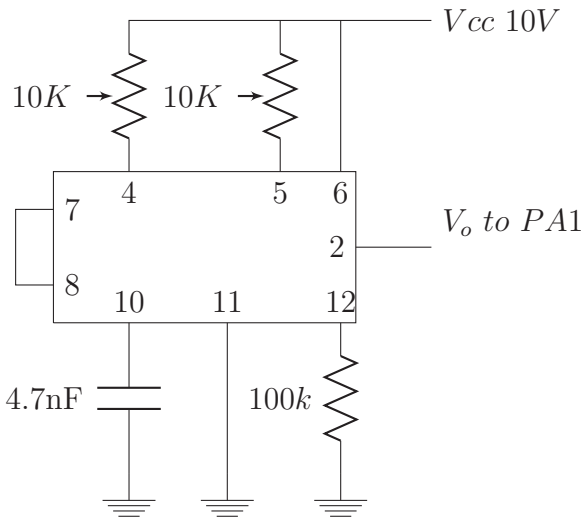


Figure 4.11: Grid Waveform Emulator Using ILC8038

4.9 Experimental Results of the Proposed Synchronisation Method

An experimental prototype was built in order to verify the suggested method. The digital microcontroller STM32F4 in ST discovery board by ST electronics was programmed with the proposed algorithm. The grid voltage waveform was fed to the ST discovery board with a help of an interfacing circuit to match the grid voltage to the controller requirement which is unipolar 3.3 Volt. System Testing was carried out to initiate the validity by checking the response speed of tracking the waveform magnitude as well as the frequency and the phase angle.

Speed response test was performed as shown in figure 4.12, lower waveform labelled $Grid\ Waveform$ mimic the fluctuation that might occur with the grid. While top trace labelled *Algorithm Response* demonstrate the prototype outcome.

Two advantages can be seen in 4.12, which are the algorithm has a high response speed to the rate of change of the grid voltage and there is a linear relation in the rate of change between the measured value and the grid voltage at low frequency variation.

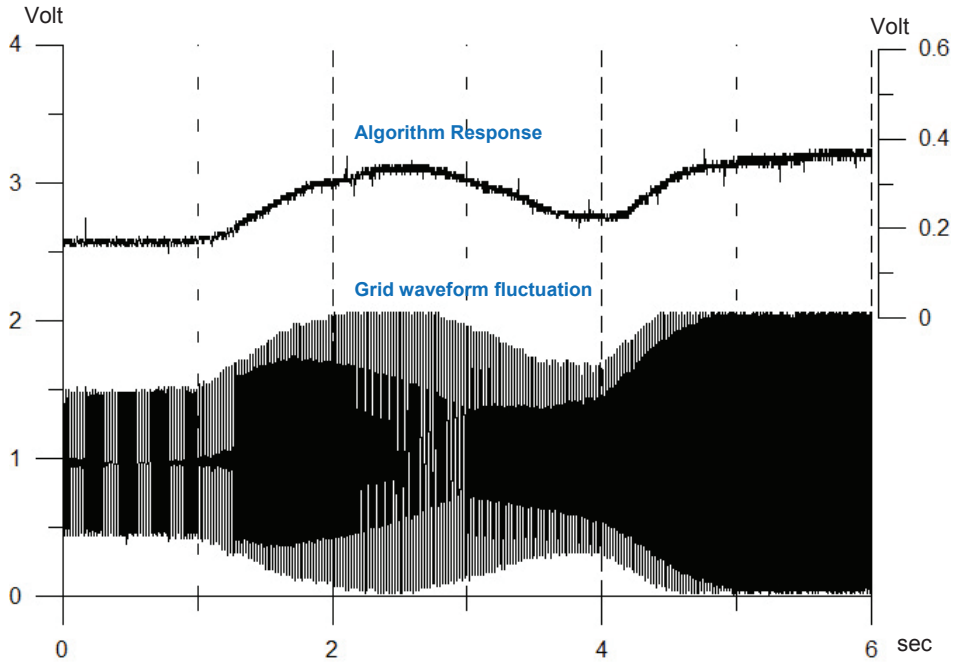


Figure 4.12: Speed Response to Input Voltage Variation

To ensure that the algorithm is able to synchronise an inverter with the grid accurately. Figure 4.13 shows a generated gate signal (pulse) of an inverter transistor that triggered at the start of each cycle of the grid waveform.

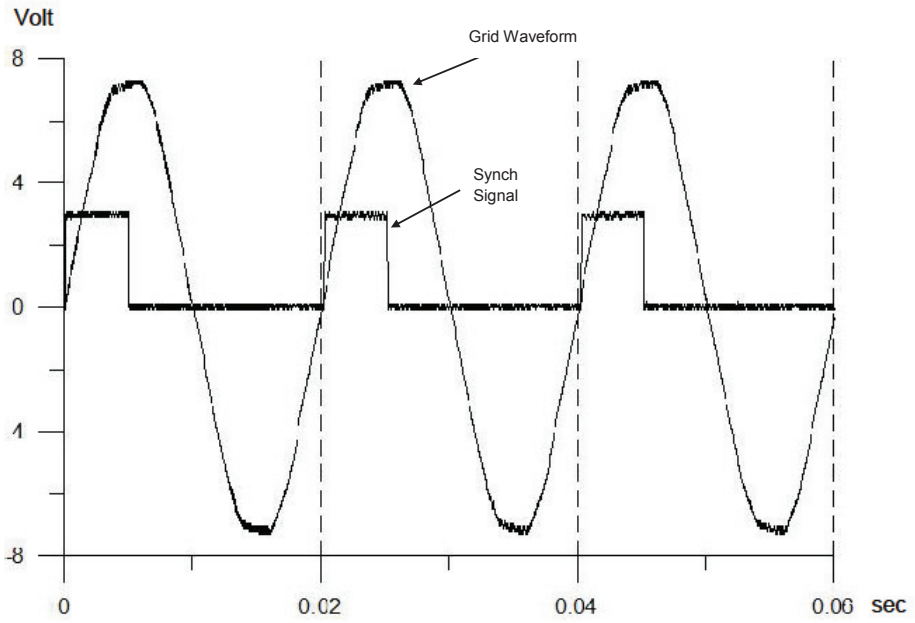


Figure 4.13: Phase and Frequency Measuring accuracy

Figure 4.14 shows that there is a missing pulse in the waveform represented by red doted square. This time is required to perform the calculations when $atan\theta$ changes from positive to negative values. In normal condition of operation there are other methods that can perform frequency tracking without missing a trigger.

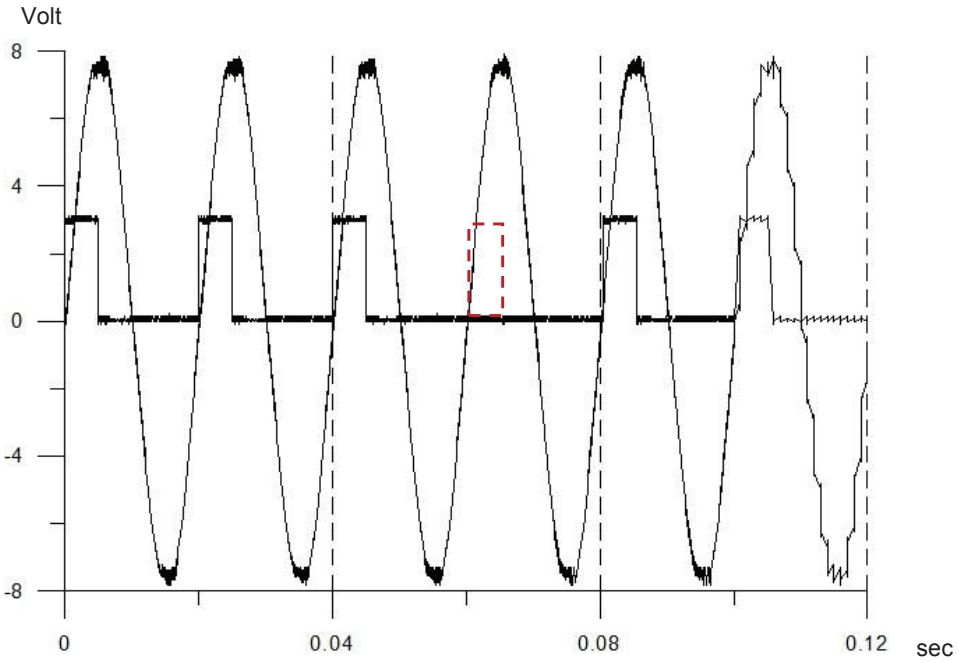


Figure 4.14: Micro-controller Resynchronisation

The micro-controller was able to generate a pulse at the start of each cycle of the fundamental component with no obvious delay shown. While the distorted sinusoidal waveform in figure 4.13 was supplied from the grid emulator to verify the proposed method.

From previous, the algorithm was able to track frequency and magnitude variation when it fed from the grid emulator through the voltage transducer. However, all tracking methods have a measurement error and experimental tests and simulation were made to find the algorithm accuracy.

The accuracy of measuring frequency and calculating phase angle is shown in figure 4.15. Where the previous figure shows experimental results of the algorithm response when fed from pure sinusoidal waveform with variable frequency. It can be seen that the error has limits of ($\mp 0.035\ Hz$). The

error is caused due to truncated waveform, where the signal period is differs than the bin width as explained in chapter two. Because the actual grid frequency varies between $49.5Hz$ to $50.5Hz$ then it can be considered that the actual error can be within the limits of 0 to (+0.025 Hz). Comparing these results to previous researches as in [79], it is clear that the error in frequency measurement made by the proposed algorithm is less than 0.17 Hz, which can verify the performance. On the other hand the proposed method has frequency detection limits between 48Hz and 52Hz which is less than [79].

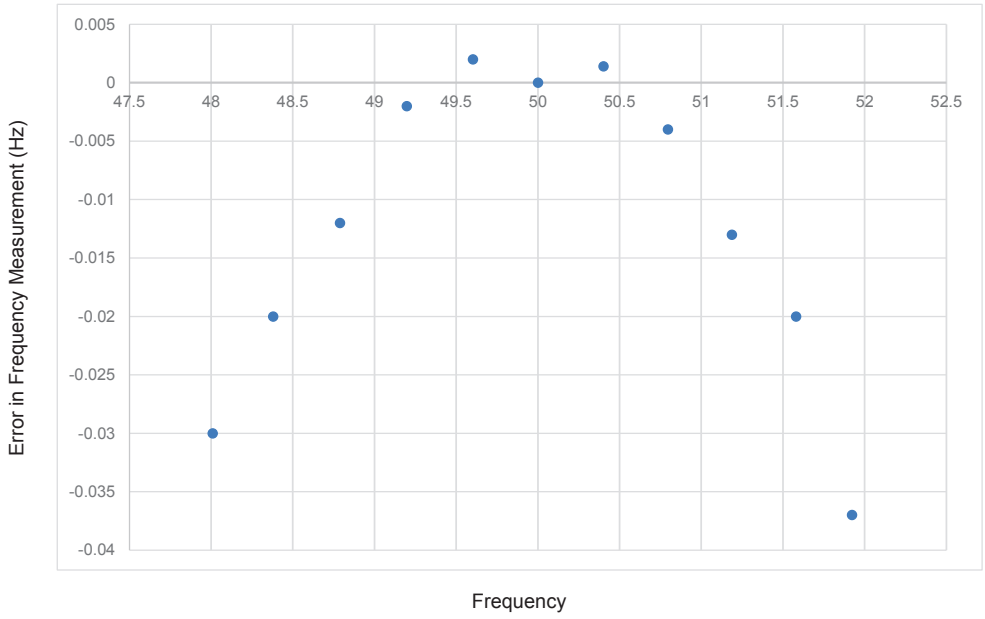


Figure 4.15: The Error in measuring the Frequency

Because calculating the magnitude relies on the measured frequency, consequently frequency measuring error will have an impact on the magnitude, as shown in figure 4.16. The highest value of the percentage error shown is limited to 0.5.

If the grid frequency is swinging between $49.5Hz$ and $50.5Hz$ during

normal operation then, the measurement error is limited to (0.25) which can be normalized.

By comparing the percentage error of measuring the magnitude to [80], it can be seen that both have the same error value 0.25 at $\mp 2Hz$ at the central frequency.

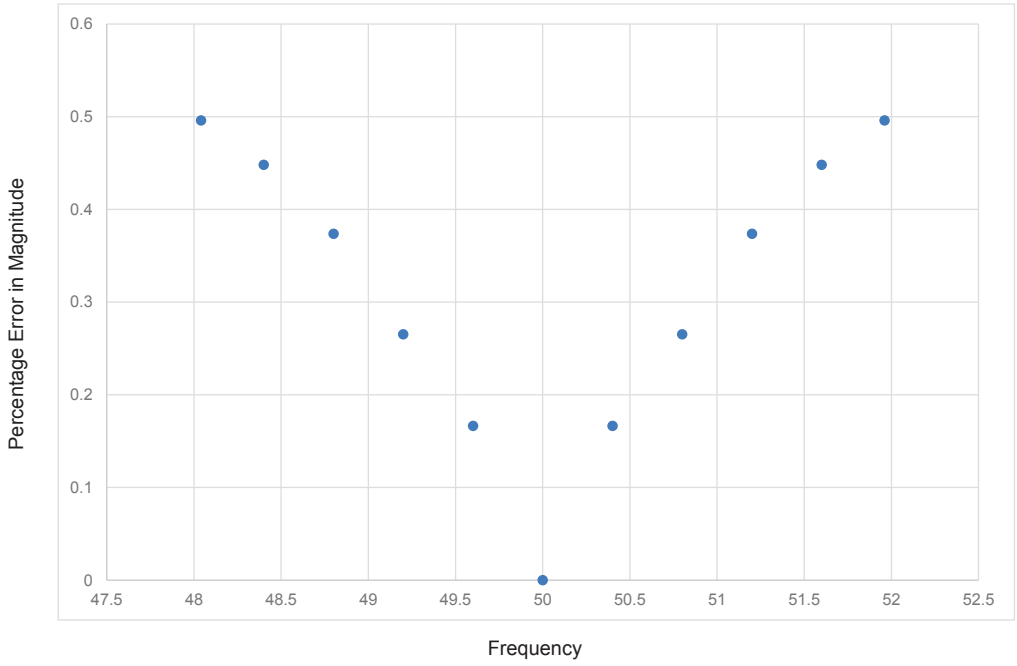


Figure 4.16: Error in Magnitude measurement VS Frequency

Figure 4.17 shows the error in calculating phase angle with respect to the measured frequency which is directly related to the algorithm execution time. It is shown that the phase error reaches (2.5°) which is within the domestic and military standard for $400V$ distribution system [81, 82] when the grid frequency is at the limits . Furthermore, the big difference in phase angle calculation is due to processing time and it is related to sampling frequency and the number of samples. During the implementation, the total number

of samples was 250 and the micro-controller was sampling at 2MHz which will cause a delay of 0.065 ms. Increasing the sampling frequency and the processing speed should lead to reduce the error in phase angle.

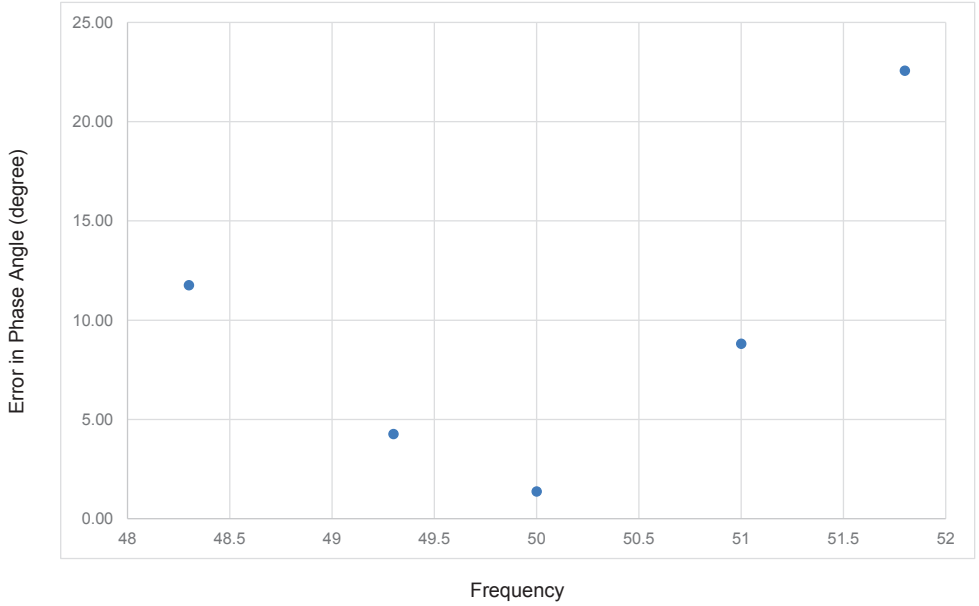


Figure 4.17: Error in Phase measurement VS Frequency

Chapter 5

Conclusion and Future Work

The importance of this work is represented by proposing an improvement on the converters in single phase DG systems. On the DC-DC converter, a new integrated structure was proposed to improve the converter voltage gain and a novel method to calculate the iron losses for the proposed structure. On the AC-DC inversion side of the DG system, a new method was proposed to improve the synchronisation of grid tie inverter.

5.1 DC converter

The proposed boost structure

High frequency transformers are an essential component in DC converters and the method of winding it can leave an impact on the performance. Where methods of winding the coils, whether inversely or directly on different limb or at the same one, will effect on the coupling coefficient and on the generated MMF.

The magnetic structure with the multiplier was successfully built and operate as an interleaved boost converter. All the windings were placed

on the central limb, this technique was suggested to improve the coupling coefficient between the windings though it has a negative impact as it concentrate the produced heat due to copper losses in one area. The new structure, improved voltage gain of the converter by factor of $2 + \eta$ which is double the voltage gain of the conventional converter if $\eta = 1$. By comparing the transfer function of the proposed structure to other research [83–85] and [86], it can be seen that the proposed work has higher gain, though it may depend on η value as well. Because the converter is controlled by changing the operating frequency, this can inject DC component to the waveform that can effect inductance of the transformer. The structure test results shows a constant value of inductance during DC bias test, which means there will no change in the inductance value during frequency changing.

Alternating the produced flux in the structure helped to increase the RMS current value due to increasing the $\frac{d\phi}{dt}$ and cancelling the effect of residual flux. Core selection and design optimization were made up with priority of chosen reducing the flux density in the core, which helped to keep the losses minimal and assist to provide high efficiency. On the other hand, because the ferrite material has parabolic losses characteristic vs temperature, the temperature was kept minimum at $43°C$ to ensure low power losses. The measured efficiency for the proposed circuit was 93%, while the magnetic structure efficiency reached 99% during no load test which affirm choosing low flux density during the design was successful.

The new method to calculate eddy and hysteresis losses Because domains of si-ferrite materials respond to the flux orientation until it reaches to a limit where the permeability of the material drops. Besides, if the flux waveform is not a single tone then all harmonics in the flux waveform will effect on domains orientation. The proposed mathematical method to find the eddy current loss will take into consideration the previous mentioned effect by applying Fourier series to find the harmonics component in flux waveform and then calculating the losses for each component. The proposed method revealed a significant difference that reaches to 20% in comparison to traditional method in iron losses calculation.

The mathematical calculations of iron loss were compared to the practical results from no-load test. the comparison showed an identical findings, which verify the method.

The importance of the improved method is noticeable at low operating frequencies on the MnZn material as that will increase the number of harmonics in the operation band.

The effect of varying the switching frequency and the duty cycle of the converter were taken into consideration, as changing the duty cycle lead to change in the magnitude of harmonics contain in the waveform.

On the other hand, applying the effect of harmonics on the hysteresis loss will not make a large change because the calculation mainly relies on flux density value rather than frequency variation.

5.2 AC Inverter

Synchronisation to a weak or distorted grid voltage with continuous frequency variation can be problematic. Usually, harmonics have its effect on the grid waveform either by changing its sinusoidal shape or by making it asymmetrical. Though the grid waveform distortion Total Harmonics Distortion (THD) should not exceed 5%, it can cause a leading or lagging in the fundamental waveform at zero-crossing point which can make many of the synchronisation method inefficient. Using DFT tool with a limited window width can extract the fundamental component from the distorted signal by filtering out all high frequencies, sub-harmonics and DC component. Applying two DFT to calculate the fundamental component by implementing it using 32 bit microcontroller was successful. The controller had been able to measure, synchronise and generate trigger in real time.

The overall system efficiency can be improved by increasing the number of samples and sampling frequency, but it is subject to the faster microcontrollers. Increasing the switching frequency can help to reduce the synchronisation angle and speeds up the response to the signal magnitude changing, while increasing the number of samples can offer a better quantization in the system.

Finally, the technique was successfully passed implemented, tested and verified. The mathematical proof demonstrates using the proposed linear approximation is accurate, which can offer a reduction in time during execution. The cost of this method is just few lines of code in comparison to PLL and ZCD.

5.3 Future Work

To improve the research, the following notes can be taken into consideration as a future work:

DC Converter To improve the DC converter gain, three phase interleave with multiplier can be investigated. The three phase converter can share one magnetic structure and distribute the phase windings on three limbs of the magnetic structure. Switches in the three phase converter will be separated from each other by $\frac{2\pi}{3}$, an overlap time can be defined as the duty cycle.

This structure will allow three periods of overlap for each 2π which can contribute to improve the voltage gain. On the other hand, spreading the windings across three limbs will maintain alternating the flux around $B-H$ curve, which contribute to reduce the magnetic structure volume.

Voltage regulation can be another important factor that can be investigated. The regulation can be improved by reducing the air-gap length and increasing the flux density. Better magnetic materials can be used to improve the efficiency by reducing the iron losses such as $N97$ and $3C97$.

Furthermore, the converter will be required to analyse as the converter gain will be affected by the operating frequency. The change in operating frequency will have an impact on the converter input impedance.

Eddy Current Analysis Though the proposed method demonstrates a significant difference in the calculation of power loss, the method can be improved by taking into consideration the change of material resistiv-

ity ρ at each frequency, though it will not cause significant difference. Another factor can have an impact on the performance, which is the demagnetization effect of the even harmonics in flux waveform, further analysis will be required to analyse even harmonics in the output current and reflect that on the demagnetization effect.

AC Inverter The proposed synchronisation method employed two RDFT to calculate the fundamental frequency in distorted signal. the number of samples in this method has an impact on the accuracy of performance, to increase the resynchronisation points, higher number of samples can be used. However, increasing the number of samples, requires using faster micro-controller to overcome the delay that occurred. On the other hand, reduce the error in phase measurement can lead to use the higher switching frequency. The method can be developed by reducing the error caused be spectrum leakage. The improvement can be done by varying the number of samples in order to match the signal frequency drift. This modification can reduce the error during the measurement Another development can be present to the proposed method is by measuring the of grid waveform. This can follow finding the grid operating frequency by changing the bin values k to measure the magnitudes of $3^{rd}, 5^{th}...n^{th}$ harmonics.

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Appendix A

Publications

The Paper was Presented and Granted Best Paper Award in the IEEE Transportation Electrification Conference and Expo Asia-Pacific 2016, Busan-Korea

A New Method to Analyse Eddy Current Loss in an Integrated Magnetic Structure for Boost Converter

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***Abstract*—This paper proposes a new integrated structure for the interleaved boost converter. The structure includes the main windings and the multipliers on the same core. A new method to calculate the eddy current loss for the used core is presented. The method takes into account the effect of the harmonics at different duty cycles on the eddy current and hysteresis losses in the core. A prototype was build and test carried out to verify the performance.**

I. Introduction

With the tendency on using renewable sources recently, providing distribution generation (DG) with low losses and high gain converters has become a need.

Improving DC converter efficiency is one of the research concerns. One of the factors that is limiting the converter's efficiency is the number of magnetics that are used per unit gain [1], where obtaining high gain requires using multi stage converters which need magnetic cores in each stage. There are many losses related the magnetic cores such as residual flux, eddy current and hysteresis. Minimizing the residual flux is considered by introducing an overlap time for the interleaved converters which will lead to an increase in the operating frequency and reduction of the core size [2]. Classically, the losses were calculated by assuming that the magnetics were supplied by a sinusoidal current waveform. [3] provides a study on the magnetic losses under biased and asymmetric excitation waveforms and compares them to sinusoidal excitation. However, the study did not cover how the asymmetrical waveform affects the losses. This paper is proposing a new single magnetic structure for interleaved boost converter with multiplier to minimise losses and analysing different factors which contribute to reducing losses. As well as proposing a new method to calculate the iron losses of the magnetics, this paper analyses the waveform shape into sub frequencies and will cover the effect of duty cycle changes in the converter.

A transformer prototype was built and tests were carried out to evaluate the performance as is covered in this paper.

II. The Proposed Structure

An adaptable interleaved DC boost circuit is shown in Figure 1 and consists of two main magnetic components and two switches and diodes. L_{in} is required to provide a current continuity during the switching overlap and to keep low current ripple on the input. The main magnetic component can be considered as a non-isolating transformer consisting of four windings, where each two in a branch construct an interleaved boost converter [4]. Both converters feed through the centre point, which is connected to the input.

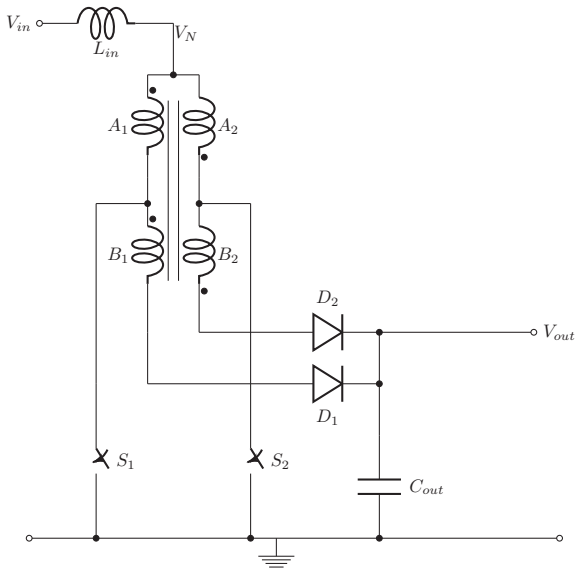

Fig. 1: Adaptable Interleaved Boost Topology

III. Flux Orientation During Operation

When switch S_1 is ON the current will flow through the A_1 windings to ground. The current will produce a flux in the core which will induce a voltage across the B_1 windings. During this operation the flux will build in one direction of the B-H curve of the magnetic core. When S_2 is ON the current will flow in the second branch through the windings A_2 to ground, leading to induce a voltage across windings B_2.

Because the windings in both branches are opposing each other, the flowing current in S_2 will induce a flux in the negative part of the B-H curve of the core material. The current waveform with the overlap operation is showing in 2

The residual flux is minimized during the operation by introducing an overlap time. During the overlap time, both switches will be closed leading to pass the current through both low voltage windings.

The current in both branches will have a different gradient and magnitude because of the residual flux in the core. This mode will cause the voltage at the centre tap of the transformer to fall to zero (or become virtual ground), therefore L_{in} is required to provide current continuity by introducing an

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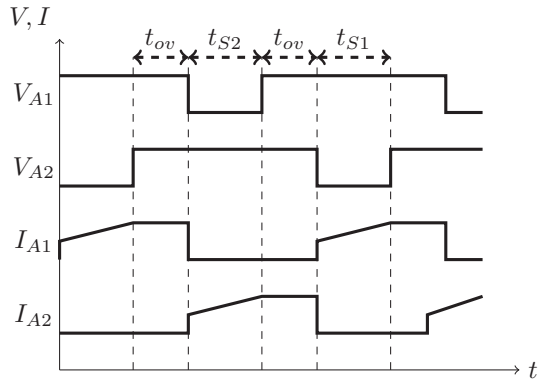

Fig. 2: Voltage and current applied to the transformer

impedance between the centre point and the source. Minimizing the residual flux will allow the operating frequency to increase to the core operating limit.

The magnetic structure will combine two interleaved boost converters, each consisting of a low voltage winding and a multiplier. This structure will minimize the number of magnetic components and should contribute to obtaining high efficiency for the topology where the losses are kept minimum.

IV. Magnetic Components

A. Core Selection

All core materials are made from a blend of selected substances and constructed in such a way to have a certain target μ. Similarly to all other components, the core permeability is subject to change due to temperature variation. The variation of the permeability has a drawback on the performance as it causes inductance variation.

Losses in magnetic components, divided into resistive and magnetic, cause power dissipation which, in turn, leads to heating of the magnetic material. The relationship of magnetic core losses as a function of temperature follow an exponential curve with an optimal point where losses are minimized at a certain temperature. The magnetic material should be kept at this temperature to maintain optimal performance. However, if heating causes the core temperature to drift away from the operating point the magnetic losses can increase significantly.

The Mn-Zn ferrite N87 has a μ of 2000 which makes it suitable for high frequency converters as the operating the flux will alternate between $200 - 600kHz$. The operating temperature will be kept at 43°C during the design [5].

B. Non-Isolating Transformer Design Consideration

Transformer design of this type of converter will require great care, where all windings should be distributed evenly across the core in order to prevent residual flux accumulation, as shown in figure 3. On the other hand, uneven coil distribution will cause a difference in the switching current, leading to an extra ripple in the output and causing a DC bias around the core hysteresis loop.

Operating the core with low flux density by having a small gap $0.1mm$ with low fringing will help to reduce the effect of the residual flux accumulation and will lead to a reduction in iron losses.

$$\frac{\int V \cdot dt}{NA} < B_{sat}$$

The number of turns of the primary windings for a non-gapped transformer core can be calculated by

$$N = \frac{V_{in}}{4 f_s B_{max} A} \tag{1}$$

Equation (1) can be used for a non-gapped core, but when a small gap is introduced the winding inductance will be reduced, leading to a mismatch in transformer impedance causing a high current magnitude to pass through the primary. However, to avoid the effect of the core gapping, the number of turns will be calculated based on the inductance value before introducing the gap.

The standard equation for inductances is

$$L = \frac{\mu A N^2}{l} \tag{2}$$

where L is the inductance, μ is the permeability, A is the cross-sectional area of the core and l is the magnetic path length (the mid-core circumference for toroidal cores). μ shown in (2) is the absolute permeability of the inductor and is comprised of μ_0 (the permeability of free space) and μ_r (the relative permeability of the magnetic material).

$$\mu = \mu_0 \mu_r$$

, μ_0 has a constant value of $4\pi \times 10^{-7}$H/m.

During the design, avoiding saturation is very important as it can occur for two reasons:

- When the flux density value exceeds B_{max} of the core ($0.5mT$ for N87), ie. when current magnitude passing through the windings produces a magnetomotive force $N \cdot i$ value that exceeds the operation point μ.
  Where
  $$B = \mu H$$
  $$B = \mu \frac{N \cdot i}{l}$$
- Due to the flux accumulation in one direction of the $B - H$ curve when there is a DC component in the current waveform.

At this point the material cannot support the magnetic characteristics and the winding will behave as a short circuit.

On the other hand, materials with lower permeability have a higher reluctance to the magnetic field, but will require more turns to achieve the target flux density. Such cores can operate at lower frequencies and switching losses can be reduced, however it will produce high copper and iron losses due to its large size.

C. Wire Selection

At high frequency $600kHz$ skin effect has a huge impact on the wire cross section. The effective skin depth can be found by [6]

$$\delta = \frac{\Delta K_{temp}}{\sqrt{f}} \tag{3}$$

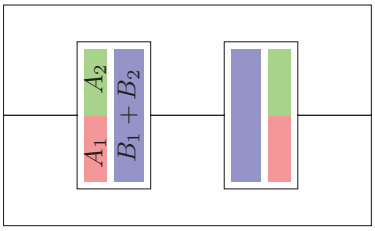

Fig. 3: Windings Distribution in the Core

where $\Delta K_{temp} = 65.5$ at $20°C \sim 72$ at $70°C$ and δ is in (mm). At the operating frequency the required diameter of the wire is 0.085mm. Taking the peak current of the primary into consideration with respect to the current density, the use of Litz wire is required at $7 \times 0.3mm$

D. transformer optimization

To achieve the high efficiency target, the transformer is optimized to have minimum copper and iron losses. Core selection is mainly based on physical size and inductance, where higher inductances are preferred to achieve a lower number of turns. However, small volume cores cannot have a high inductance, leading the design to have higher turns which means higher copper loss and less iron loss. The design optimization is to find a point where both losses have the same value by taking into consideration the core power handling capability and mechanical limitation that can be obtained by equation 4.

$$W_a A_c = \frac{Po \cdot K}{B_m \cdot f_s} \tag{4}$$

where W_a is the window area of the core, A_c is the core cross section area, P_o is the total power carried by the core. Due to litz wire size, winding number will limit the core volume to $7640mm^3$ using ETD-34

V. Magnetic Losses

The losses in the magnetic components of the converters are divided into copper and iron losses. There are different factors that affect loss values, such as:

- Operating frequency
- Core size and material
- Flux density
- Operating temperature

In this paper the shape of the current waveform will be considered as a factor which affects both copper and iron losses.

A. Loss Caused by Magnetics

A voltage will be induced across the ferrite grains when a rate of change of flux exists in Mn-Zn ferrite material produced by a current passing through the windings. Because the grains have a specific resistivity R_g, it will allow a certain amount of current to pass through the bounded grains. This current is known as an eddy current.

At higher frequency there is another effect which will appear across the boundary layers between the grains. This effect will be presented as a capacitance C_b. This will cause an extra loss in the material because of shorting the layer [7] at high frequency.

The slow response of the grains to the flux changing can cause another type of loss in the core as hysteresis because it will require more energy to force the segment to change polarity. Both components are iron losses and are subject to the core size, core material, frequency and waveform shape at constant temperature.

$$P_e = K_e \cdot f_s^2 \cdot B_m^2 \cdot \frac{A_c}{\rho} \tag{5}$$

$$P_h = K_h \cdot f_s^x \cdot B_m^y \tag{6}$$

Where K_e and K_h are the eddy current and hysteresis constants, A_c is the material cross section aria, x is 1.64 and y is 2.68 for the material N87. While residual losses is

$$P_{resd} = 0.12\ Tesla$$

will be considered as a constant [5].

B. Proposed Method to Find Magnetic Losses

Because the losses are linked to the frequency and flux density, the classic way of calculating the core iron losses [8] will be accurate when a single tone current produces a flux. Research has been published to analyse the magnetic losses. However, this research considered the operating frequency as a pure sinusoidal waveform [9], [10], while Mn-Zn cores are usually used with switching power supplies which produce asymmetrical waveforms which contain harmonics.

In power electronics converters most of the magnetic materials are supplied with square or trianguler current waveforms with variable duty cycle. This will excite a flux in the core at different frequencies.

$$B(t) = B_{dc} + \sum_{n=1}^{\infty} Bm_n \cdot sin(w_n t) \tag{7}$$

Where n is odd integer

Because the current waveform as shown in figure 2 has an approximate square shape and the flux density is chosen to have a small value, the produced flux in the transformer core will have the same shape. The expected flux waveform shown in figure 4 is a bipolar square wave that has a zero magnitude depending on the duty cycle.

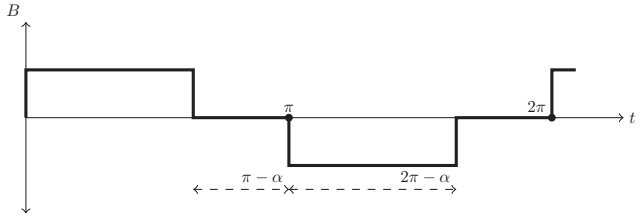

Fig. 4: Flux Waveform in the Transformer

$$B(avg) = \frac{2}{\pi\ A_c}\left(\int_0^{\pi-\alpha} \phi\ dt\right) \tag{8}$$

By finding the odd harmonics in the waveform, we will have:

$$B(\omega) = \frac{2}{\pi\ A_c}\left(\int_0^{\pi-\alpha} \phi.sin(n\cdot\omega t)dt\right) \tag{9}$$

The flux in the core has two components, imaginary and real, both of which will vary with respect to the field frequency. Because eddy current loss is caused only by the real component of the flux, it can be calculated thus

$$B(n) = \sum_{n=1,3,5}^{Q}\left(\frac{2\cdot B_{peak}}{n\pi}\left(1-cos((\pi-\alpha)n)\right)\right) \tag{10}$$

where Q is the factor that is limited by the material highest operating frequency.

By substituting equation 10 in 5 and assuming the material MnZn resistivity, ρ, is constant from n=1 to Q, the effect of all harmonics and duty cycle changing on eddy current loss will be:

$$P_e(n) = K_e \sum_{n=1,3,5}^{Q} \cdot f_n^2 \cdot \left(\frac{2\cdot B_{peak}}{n\ \pi}\left(1-cos((pi-\alpha)n)\right)\right)^2 \frac{A_c}{\rho} \tag{11}$$

C. *Effect of high frequency operation on ferrite permeability*

The ferrite material responds differently at different frequencies due to the increase in the imaginary part of the permeability μ'' leading to an increase in the loss factor $tan\ \delta$ [11]. where

$$tan\ \delta = \frac{\mu''}{\mu'} \tag{12}$$

$$\mu = \mu' - J\mu''$$

VI. Results and Discussion

The total iron loss of the core is 1.9 $watt$ for a 200 $watt$ system. This provided an efficiency of 99% excluding the copper loss to the prototype. According to the figure 5 obtained from the prototype test, it can be seen that the area under the waveform curve has an average value of zero, which means that the windings are evenly distributed in the core. This will prevent flux accumulation in any direction of the B-H curve, leading to saturation. Figure 6 shows the current waveform of the A windings which has the same rate of change as the flux waveform but unipolar.

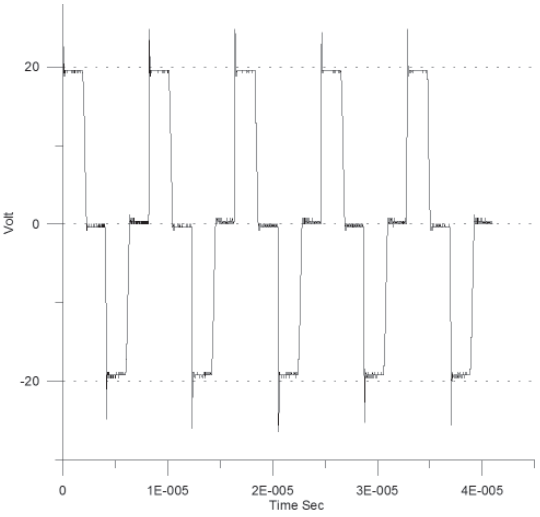

Fig. 5: Flux waveform in the core

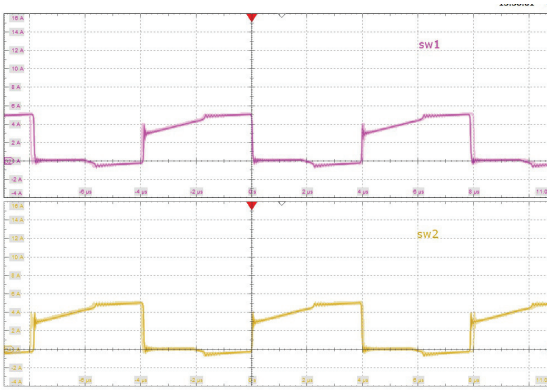

Fig. 6: Current waveform of the A windings

The design priority is to have flux density of 0.015 $Tesla$ to ensure reduction in the iron losses. Figures 7 and 8 show the optimum frequency and the number of turns for the 0.16mm gapped core based on the calculations.

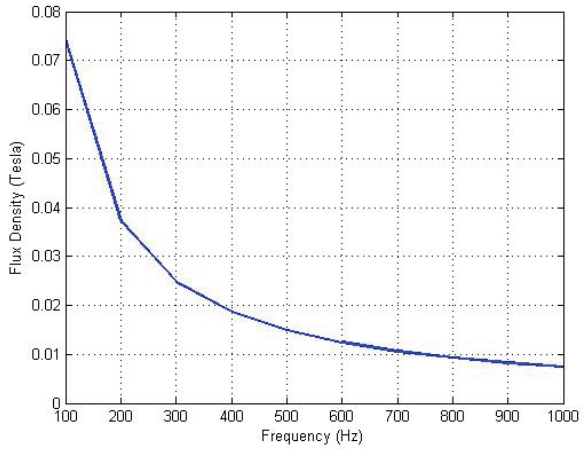

Fig. 7: Flux Density at Different Frequencies

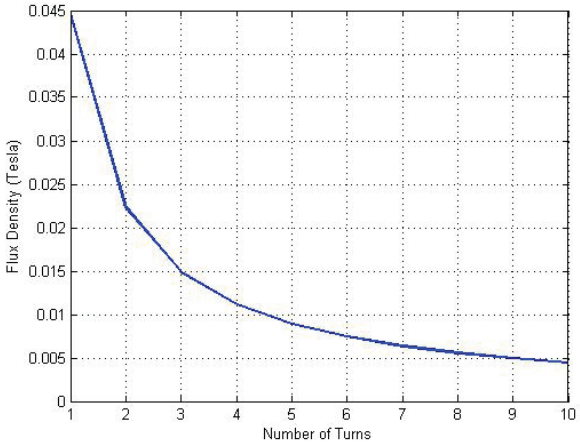

Fig. 8: Flux Density at Different Number of Turns

Figure 9 shows the simulation result of the expected eddy current loss per volume. The quasi square flux waveform is analysed at different α where $\alpha = \pi - DutyCycle$. The eddy current loss is then calculated for each harmonic and added to the main loss of the fundamental component. The total loss increased by 20% at $\alpha = 0$, while it reaches 37% at $\alpha = \frac{\pi}{2}$.

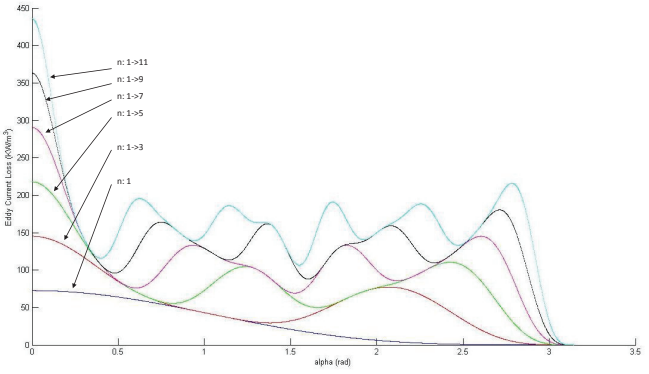

Fig. 9: Eddy Current Loss VS α with respect to Different number of harmonics

Hysteresis loss is also considered the harmonics caused by changing α. Figure 10 shows the simulation result of the effect of harmonic components on the loss, where the total hysteresis loss increased by 22%. However the loss for $\alpha > 1.5\ rad$ is not significant.

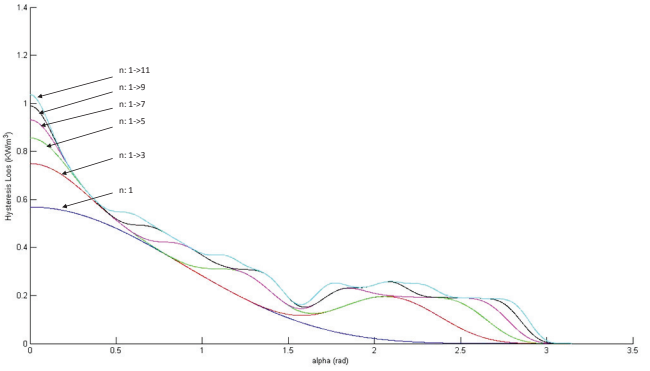

Fig. 10: Hysteresis Current Loss VS α with respect to Different number of harmonics

VII. Conclusion

The proposed magnetic structure with the multiplier was successfully built to operate as an interleaved boost. Combine both winding branches on the same core and reducing the flux density during the design helped to keep the losses minimal which provides high circuit efficiency. The new method to calculate the eddy current loss shows a significant difference that reaches to 37% in comparison to the traditional method. The importance of the improved method to calculate the eddy current can be more noticeable at lower operating frequencies with MnZn material. On the other hand applying the effect of harmonics on the hysteresis loss will not make a large change because the calculation mainly rely on flux density value.

Acknowledgement

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An Adaptable Interleaved DC-DC Boost Converter

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***Abstract*—A new topology for an interleaved boost converter is presented in this paper. The circuit is able to provide high voltage gain without the need for using a large duty cycle. Analysis showing the effect of increasing inductor winding loss in relation to duty cycle is also presented. Losses in various components are considered and analysed. Finally, experimental results from a 200W prototype which was used to boost 25V to 300V are presented and verified the design.**

I. Introduction

One of the largest difficulties encountered during voltage boosting is when attempting to achieve efficient high-power output with a high voltage gain using single stage Boost converter. Although tapped Boost converters can be considered as one of the high efficiency DC power transformers, it still faces a problem of efficiency reduction at large duty cycles [1], [2]. The duality principle of using two converters has been investigated by [3], and an interleaved Boost converter architecture was proposed. This type of converter has high current handling capability, and it has been used in different applications [4], [5]. Using an inter-phase transformer to control the converter in current mode by sensing the current through the transformer, and driving the opposite switch has been suggested as a method of improving the converter [6]. Improving voltage gain by adding a multiplier was suggested by [7] and it also contributed towards improving the overall efficiency.

This paper proposes an architecture that combines a multiplier and an interleaved boost converter topology to extract the advantages of each. The voltage transfer function of the new topology has been derived, and a prototype has been built. Findings from various tests are presented, supporting the theoretical results.

II. The Proposed Circuit Description

The proposed circuit is shown in Figure 1 which consists of two independent magnetic components and four switches (two controlled switches, S_1 and S_2; and two diodes, D_1 and D_2). Switches S_1 and S_2 are operated using a suitable control system with a degree of overlap in switching time, while the diodes are used to prevent reverse conduction current. L_{in} is required to maintain a low current ripple at the input respectively. C_{out} is used to maintain a steady output voltage, V_{out}. The main magnetic component plays a major role in circuit operation and provides some voltage boosting. Using this, high voltage gain can be obtained by increasing the turns ratio while keeping the duty cycle relatively small. The main magnetic component can be considered as a non-isolating transformer with five taps; the centre point is connected to the input and two identical tapped inductors that complement each other. During circuit operation; the two switches are used to alternate the flux in the core, producing an alternating current at the output points which is rectified by the diodes.

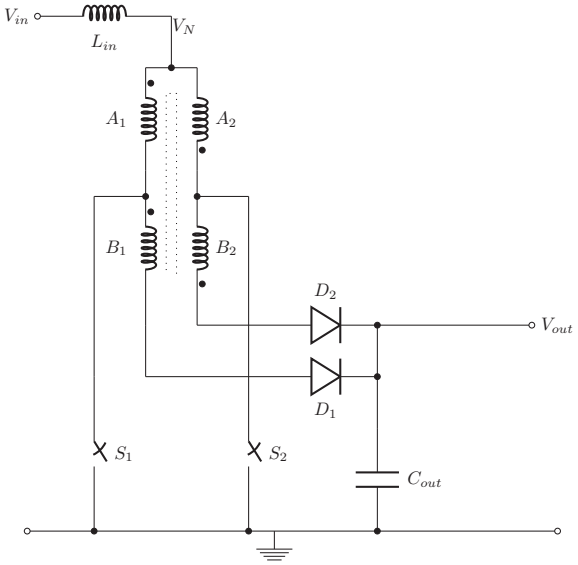


Fig. 1: Proposed Boost Topology

III. Steady State Voltage Transfer Function

The proposed circuit has two states of operation. The first when both switches are closed and the second when only one switch is closed and the other is open, as shown in Figure 2

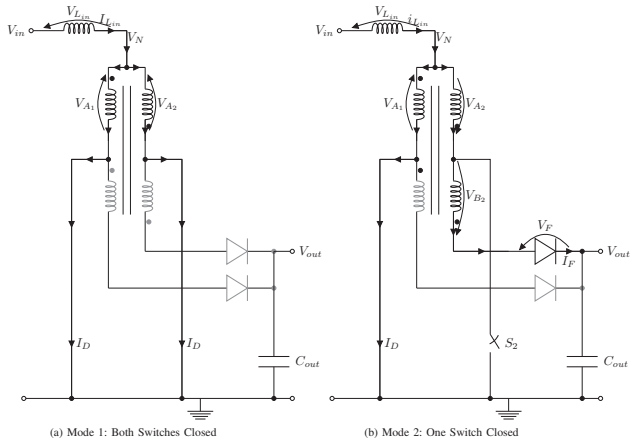
Assuming the windings A_1 and A_2 are identical and also assuming the windings B_1 and B_2 are identical; then $V_{A_1} = V_{A_2} = V_A$ and $V_{B_1} = V_{B_2} = V_B$. The transfer function can be derived by analysing the two operating states.

1) Both Switches Closed: With both switches closed during t_{on}, the node voltage V_N as shown in Figure 2a, is virtual ground because

$$V_N = V_A - V_A = 0$$

This means the potential difference across L_{in} is equal to V_{in}, leading to

$$V_{in} = L_{in}\frac{\Delta i_{L_{in}}}{\Delta t}$$



(a) Mode 1: Both Switches Closed (b) Mode 2: One Switch Closed

Fig. 2: Modes of Operation

Defining the duty cycle as

$$D = \frac{t_{on}}{T} \tag{1}$$

where T is the switching period and t_{on} is the time where both switches are closed, we can evaluate the change in current as

$$\Delta i_{L_{in}} = \frac{V_{in} DT}{L_{in}} \tag{2}$$

2) One Switch Closed: During the period where only one switch is closed, as shown in Figure 2b, the potential difference across L_{in} is given by

$$V_{L_{in}} = -(V_{in} - V_N)$$

The output potential is then given by

$$V_{out} = 2V_A + V_B \tag{3}$$

Assuming

$$\frac{V_B}{V_A} = \eta$$

we then get

$$V_{out} = V_A (2 + \eta)$$

from which

$$V_A = \frac{V_{out}}{2 + \eta} \tag{4}$$

Observing that in this mode $V_N = V_A$, and using (4), we get

$$V_{L_{in}} = -\left(V_{in} - \frac{V_{out}}{2 + \eta}\right) = L_{in} \frac{\Delta i_{L_{in}}}{(1 - D)T}$$

Rearranging this for $\Delta i_{L_{in}}$ gives

$$\Delta i_{L_{in}} = \frac{-\left(V_{in} - \frac{V_{out}}{2+\eta}\right) T(1 - D)}{L_{in}} \tag{5}$$

During steady state operation, (2) and (5) are equal, from which it can be shown that

$$\frac{V_{out}}{V_{in}} = (2 + \eta) \frac{1}{1 - D} \tag{6}$$

This transfer function is comprised of both the classic boost transfer function $\frac{1}{(1-D)}$, and a scaling factor of $(2+\eta)$. Figure 3 shows this transfer function as a function of D and η. From Figure 2b, the maximum blocking potential difference across the controlled switches is $2V_A$ and the maximum blocking potential across the diode is $V_{out}+V_B$. This enables the choice of appropriate components, and also leads to the controlled switches having a lower blocking potential compared to the diodes, permitting the use of devices with high current capability and lower on resistance.

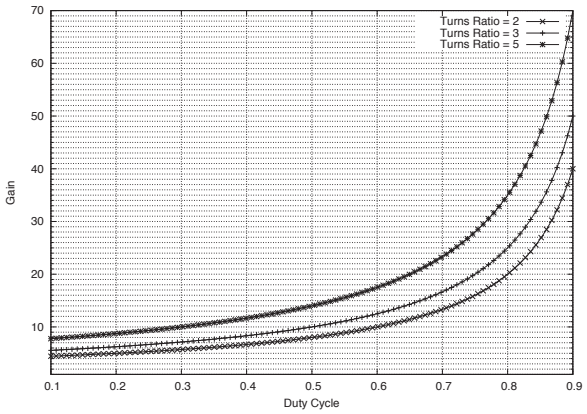


Fig. 3: Proposed Topology Voltage Gain vs Duty Cycle at Different Turns Ratio

IV. Circuit Losses

The electrical losses in this converter are distributed across the switching components and the windings as follow

A. MOSFET Losses

To find the losses associated with a single MOSFETs, the conduction period of each over a switching time T should be defined. The timing waveforms shown in Figure 4 can be used

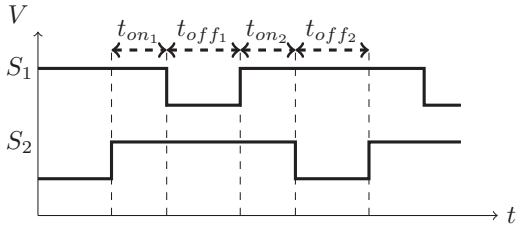


Fig. 4: Switch Timing Waveforms of S_1 and S_2

to clarify the conduction time of S_2 as follows. Defining the switching period of S_2 as

$$T_{S_2} = t_{on_1} + t_{off_1} + t_{on_2} + t_{off_2}$$

and the conduction period as

$$t_{on_{S_2}} = t_{on_1} + t_{off_1} + t_{on_2}$$

The effective duty cycle of the switch D_{S_2} can be expressed as

$$D_{S_2} = \frac{t_{on_{S_2}}}{T_{S_2}}$$

Because the switching pattern is identical for both switches S_1 and S_2, we can assume

$$t_{on_1} = t_{on_2} = t_{on} \text{ and, } t_{off_1} = t_{off_2} = t_{off}$$

from which

$$T_{S_2} = 2t_{on} + 2t_{off}$$

and

$$D_{S_2} = \frac{2t_{on} + t_{off}}{T_{S_2}}$$

From (1), $D = \frac{2t_{on}}{T_{S_2}}$ therefore $\frac{2t_{off}}{T_{S_2}} = (1 - D)$, and

$$D_{S_2} = D + \frac{1 - D}{2}$$

simplifying which gives

$$D_{S_2} = \frac{1 + D}{2} \tag{7}$$

The power loss in the MOSFET is generated from three parameters

1) **Conduction Losses** The conduction loss of the device, P_c, is given by

$$P_c = I^2_{D_{rms}} \; R_{DS_{on}} \; D_{S_2} \tag{8}$$

where $R_{DS_{on}}$ is the Drain-Source on resistance of the device.

2) **Switching Losses**
Figure 6 shows an approximate waveform of drain current i_D for a MOSFET during the switching transient.

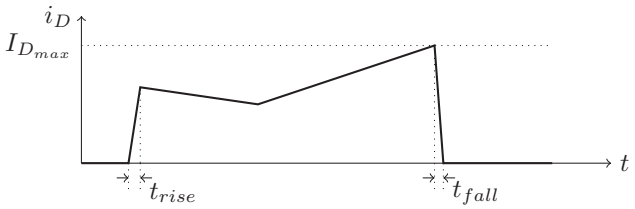


Fig. 5: i_D Timing Diagram

Fig. 6: Timing Diagrams for Rising and Falling Drain Currents

Using straight line approximations of the transient time, the total energy loss during switching, E_s, can be upper bounded by using V_{DS} which is a constant, and the maximum value of the drain source current, $I_{D_{max}}$ as

$$E_s = \int v(t)i(t) \text{ dt} < V_{DS}\frac{I_{D_{max}}}{2} \; (t_{rise} + t_{fall})$$

from this

$$P_s < V_{DS}\frac{I_{D_{max}}}{2}\frac{(t_{rise} + t_{fall})}{T} \tag{9}$$

3) **Reverse Recovery Loss**
When one MOSFET switches off, reverse conduction current i_{rr} flows in the opposite direction through the MOSFET as it re-establishes its inversion layer. Even though i_{rr} is very small it occurs at a time when V_{DS} is very high so the power loss is still significant. The total charge Q_{rr} contained in this process is given as

$$Q_{rr} = \int_0^{t_{rr}} i_{rr}(t) \text{ dt}$$

where t_{rr} is the Reverse Recovery Time.
The power dissipated is given by

$$P_r = \frac{1}{T} \cdot \int_0^{t_{rr}} i_{rr}(t) \cdot v_{rr}(t) \text{ dt}$$

$v_{rr}(t)$ is a constant value of V_{DS} so we get

$$P_r = \frac{V_{DS}}{T} \cdot \int_0^{t_{rr}} i_{rr}(t) \text{ dt}$$

This leads to

$$P_r = \frac{V_{DS}}{T} Q_{rr} \tag{10}$$

When all the above characteristics are combined, an upper bound to the total loss in the MOSFET over an entire switching period T is given by

$$\begin{aligned} P_m &= P_c + P_r + P_s \\ &= I^2_{D_{rms}} \; R_{DS_{on}} \; D_{S_2} + \frac{V_{DS}}{T} Q_{rr} \\ &\quad + V_{DS}\frac{I_{D_{max}}}{2}\frac{(t_{rise} + t_{fall})}{T} \end{aligned}$$

This the previous expression can be rewritten in terms of V_{out}, as

$$\begin{aligned} P_m &= I^2_{D_{rms}} \; R_{DS_{on}} \; D_{S_2} \\ &\quad + \frac{2V_{out}}{(2+\eta)T}\left[Q_{rr} + \frac{I_{D_{max}}}{2}\,(t_{rise} + t_{fall})\right] \end{aligned} \tag{11}$$

B. Diode Losses

To improve efficiency, Silicon Carbide (SiC) diodes were used in order to eliminate the reverse leakage losses that are associated with silicon diodes. Thus the main significant loss to consider is the diode conduction loss.

By applying a straight line approximation to the characteristic curve of the device, and using a threshold voltage V_{T0} and the impedance R_D, the loss in the diode can be written as a function of the average current, $I_{F_{av}}$, and the RMS current, $I_{F_{rms}}$, through the diode as

$$P_d = V_{T0} \cdot I_{F_{av}} + R_D \cdot I^2_{F_{rms}} \tag{12}$$

C. Winding Losses

When dealing with high power at low voltage, the power losses in the conductors can be very high due to the large current and also the harmonic content [8]. Each frequency component, f_i, produces a certain amount of flux around the wire that is proportional to its value. Each component also has a unique skin depth δ_i related to the its frequency, normally estimated for Copper wire as $\delta_i = \frac{6.62}{\sqrt{f_i}}$ cm where the frequency is specified in Hz.

The current in the windings is an asymmetric traingular waveform with a ripple of I_r and a DC value, I_{DC} as shown in Figure 7.

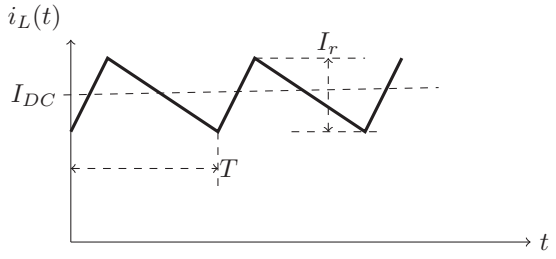


Fig. 7: L_{in} Current

The expression of this waveform is given by [9] as

$$i_L(t) = I_{DC} + \sum_{n=1}^{\infty} \left[(-1)^{(n-1)} \frac{I_r}{\pi} \frac{\text{sinc}\left((1-D)n\right)}{Dn} \right] \sin\left(2\pi n f_1 t\right) \quad (13)$$

where $f_1 = \frac{1}{T}$ and is the switching frequency of the converter and

$$\text{sinc}(x) = \begin{cases} 1 & \text{if } x = 0 \\ \frac{\sin(x\pi)}{x\pi} & \text{otherwise} \end{cases}$$

The RMS value of the Fourier component at f_n is given by

$$I_n(D) = \frac{I_r}{\pi\sqrt{2}} \frac{\text{sinc}\left((1-D)n\right)}{Dn}$$

The total winding losses can be calculated by taking into consideration all the current components [8]. The DC component of $i_L(t)$ will not be affected by the duty cycle, and hence the DC resistance loss is a constant. However, the harmonics will be affected as described by the equation below,

$$P_h(D) = \rho l \sum_{n=1}^{\infty} \frac{(I_n(D))^2}{A(nf_1)} \quad (14)$$

where $A(nf_1)$ is the cross-sectional area based on the skin depth at harmonic n, l is the length of the wire and ρ is the resistivity of the material. Equation 14 can be employed to find the wire losses in L_{in} by limiting the summation to a finite number of harmonics. From (14), the variation of loss due to the duty cycle can be computed and is a minimum when $D = 0.5$. A Duty Cycle Factor, $F(D)$ can be defined as

$$F(D) = \frac{P_h(D)}{P_h(0.5)}$$

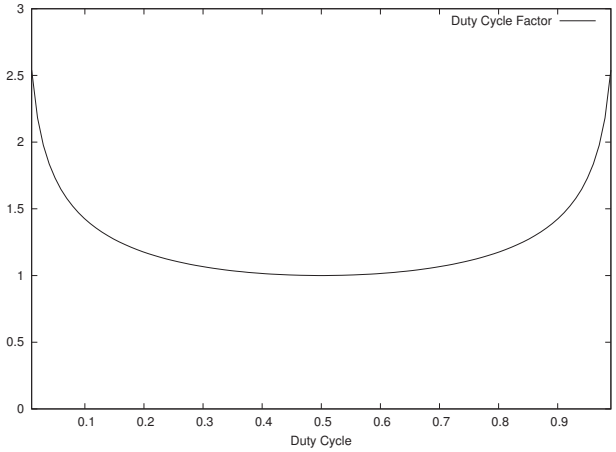


Fig. 8: Duty Cycle Factor

shown in Figure 8

From this figure, in order to keep the losses low, the duty cycle needs to be kept within a range of 0.2 to 0.8 from a practical perspective.

V. Experimental Results

An experimental circuit was built and tests were carried out to verify the performance. The prototype supplied a constant voltage load of 300 V, fed from a variable source ranging from 25 to 50 V. Details of the used components are shown in table I.

Device	Parameter	Value	Unit
Input Voltage	V_{in}	25$\leq V_{in} \leq$50	V
Turns ratio	η	3	
DC Resistance	R_{DC}	38	mΩ per m
Length	l	0.15	m
Frequency	$\frac{1}{T}$	200-300	kHz
MOSFET's S_1, S_2	V_{DS} Rating	$\geq$120.0	V
	$R_{DS(on)}$	80.0	mΩ
	Q_g	114.6	nC
Diodes D_1, D_2	V_{T0}	1.2	V
	R_D	75	mΩ
	V_{RRM} Rating	$\geq$480	V

TABLE I: Experimental Circuit Parameters

A power handling capability of 200 W was reached while the circuit efficiency exceeded 92% during full-load condition as shown in Figure 9. The main loss was attributed to the MOSFETs, which had an $R_{DS_{on}}$ of 80mΩ passing 8A of current. Using lower $R_{DS_{on}}$ devices can enable an efficiency of 96%.

The switch voltage V_{DS} and its current I_{DS} is shown in Figure 10. This figure shows the maximum reverse voltage across the switch being equal to $2V_A$. It also shows the turn on current (and consequently turn on loss), which is overestimated as in equation (9).

Voltage and current waveforms associated with the SiC diodes are shown in Figure 11. The maximum blocking

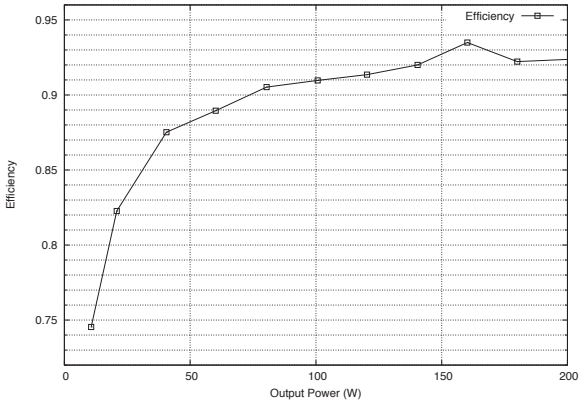


Fig. 9: Experimental Circuit Efficiency

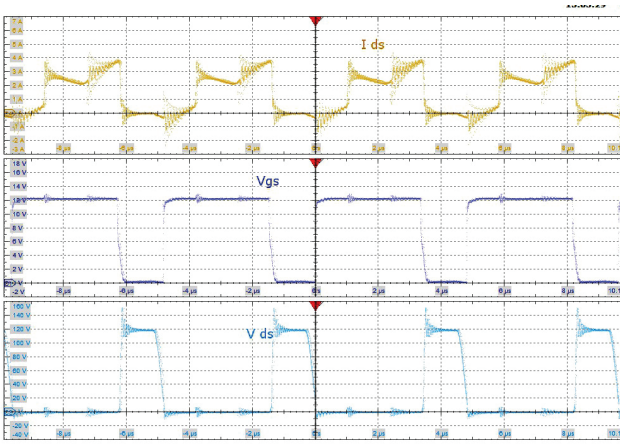


Fig. 10: MOSFET I_{DS}, Gate Signal V_{gs}, and V_{DS}

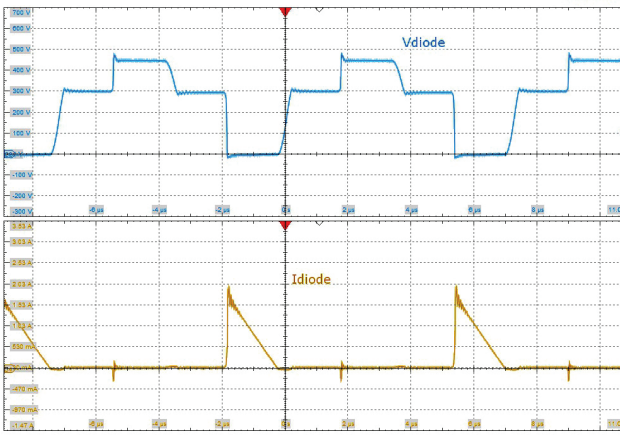


Fig. 11: SiC Diode V_d and I_d Waveform

potential of the diode is verified as V_B+V_{out}, and two blocking regions are clearly identified. The diode normally blocks V_{out} when both S_1 and S_2 are closed. When one switch is open, the diode associated with the other switch then blocks $V_B + V_{out}$.

The current in L_{in} is presented in Figure 12. This shows

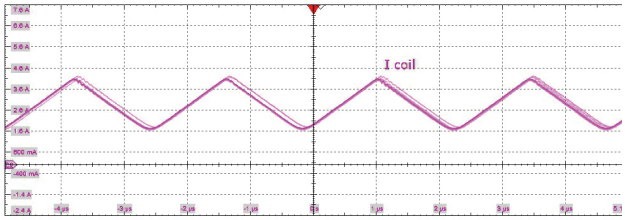


Fig. 12: Measured $i_L(t)$

good agreement with the ideal waveform shown in Figure 7.

VI. Conclusion

This paper presents a new topology for boosting DC voltage. The topology achieves a high gain due to the factor $(2+\eta)$ that is related to the tapped transformer. Due to the $(2+\eta)$ factor, a smaller duty cycle is needed to achieve the same gain when it compared to the conventional boost converter. Introducing the overlap during switching reduces the voltage and current stress on the MOSFETs which improves efficiency and enables the use of lower rated components. The effect of duty cycle on copper loss has also been presented, with the minimal copper loss occuring when the duty cycle is 0.5

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A New Method for Grid-Tie Inverters Synchronization Based on RDFT with Linear Approximation

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***Abstract*—A new method based on linear approximation of RDFT is presented in this paper which will provide a computation reduction as well as high accuracy in tracking the fundamental in distorted grid during synchronization. Due to recent developments combined with the increasing of power demand by single phase nonlinear loads, voltage spikes, harmonics and DC component had affected on the electric grid quality. These effects make Synchronization a challenge where filters or DSP analysers are required to acquire the fundamental component as a consequence to the waveform deformation.**

Applying DFT "Discrete Fourier Transform" using DSP processors can be one of the best solutions to find the waveform parameters. However DFT is combined with high mathematical computations and required using advanced microprocessors to be applied in real-time.

I. Introduction

Increasing The grid diversity by connecting different type of loads and power sources in parallel made the synchronization process is challenge due to waveform distortion. Synchronising source with the grid requires measuring the voltage phasor accurately in real time to perform synchronization. There are many techniques that can be used to perform phasor synchronization, such as using phase locked loop (PLL) [1],Zero Crossing Detector, Discrete Fourier Transform (DFT) in digital systems and modified zero crossing detector [2]. Generally, digital PLL's are low in reliability when there is a DC component in the grid waveform and that due to device saturation and losing lock [3],while zero crossing detector cannot estimate the fundamental if the signal contain harmonics. Therefore, DFT is becoming more widely used in analysis of fundamental component and harmonics of electric utility voltage and current [4].

Basically healthy grid voltage is a single tone waveform and it can be represented as

$$V_g = V_m \cdot \sin(\omega t + \theta) \tag{1}$$

while the previous equation can be rewritten when the voltage waveform is distorted by the sum of fundamental and h number of odd harmonics

$$V_g = V_{dc} + \sum_{h=1}^{h=\infty} \frac{V_m}{h} \cdot \sin((h \cdot \omega t) + \theta) \tag{2}$$

Where V_{dc} is the DC component in the grid

Referring to equation (1), there are three variables which are the fundamental voltage magnitude Vm, frequency ω and phase θ that should be measured precisely in order to synchronize to the grid. Finding the true Root Mean Square (RMS) value can be easily done when the waveform is sinusoidal, while it can be long process when the waveform is distorted or in weak condition. Previous research Have investigated synchronization to grid under abnormal condition of operation such as [5] was able to combine the effect of the transient process of the grid by adding a DC factor. [6] presented two techniques, one relying on the DFT window width by matching it to the period of the signal while the second was relying on calculating the phase offset by comparing it to known phase. In research [7] was also focusing on estimation of phase angle based on calculating the phase error of positive sequence of three phase system. Calculating the effective admittance in frequency domain and estimating the frequency was presented in [8] while [9] estimate admittance by decomposition the current waveform using RDFT.

II. Discrete Fourier Transform

DFT is an essential tool in digital signal processing that can be implemented to obtain the fundamental signal parameters by filtering the grid voltage waveform and it can be described as follows.

$$V_k = \sum_{n=0}^{N-1} v_n \cdot e^{-j2\pi n \frac{k}{N}} \tag{3}$$

where $k = 0, 1, 2, \cdots, (N-1)$;Fourier Transform bin

N: total number of the samples taken at a sampling frequency.

v_n: the sampled voltage

Referring to the equation (3) DFT operates by sampling the input signal by f_s frequency to calculate the component of

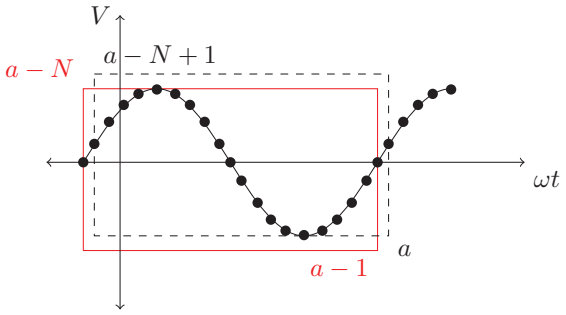

Fig. 1. sampling window width

certain frequency (fg). Bin-width or frequency resolution can be found by stating the number of samples (N) as shown in Fig.1.

where:

$$binwidth = \frac{f_s}{N} \tag{4}$$

Grid waveform in equation (1) can be rewritten in complex notation as follow [4]

$$\overline{V} = Ve^{-j\theta} = V\cos\theta + jV\sin\theta \tag{5}$$

by substituting equation (5) in (3) the voltage phasor can be represented as real and imagery component as follows:

$$\Re_e V[k] = \sum_{n=0}^{N-1} v_n \cos\left(2\pi n\frac{k}{N}\right) \tag{6}$$

$$ImV[k] = -\sum_{n=0}^{N-1} v_n \sin\left(2\pi n\frac{k}{N}\right) \tag{7}$$

III. Recursive Discrete Fourier Transform

The RDFT has been developed at first to simplify the computational complexity of DFT since then it was widely employed in frequency detection and phasor calculations.

According to [10] RDFT has been one of the fastest algorithms in power system application because it is computationally efficient. RDFT can be used to find the value of V_k for a constant k.

$$V_{k-1} = \sum_{n=a-N}^{a-1} v_n \cdot e^{-j2\pi\frac{n-1\cdot k}{N}} \tag{8}$$

$$V_k = \sum_{n=a-N+1}^{a} v_n \cdot e^{-j2\pi\frac{n-1\cdot k}{N}} \tag{9}$$

Thus

$$V_k^{NOW} = V_{k-1}^{PREV} - v_1 \cdot e^{\frac{-j2\pi n}{N}} + \cdots + v_N \cdot e^{\frac{-j2\pi nk}{N}} \tag{10}$$

it can be simplified to

$$V_k^{NOW} = V_{k-1}^{PREV} + (v_n - v_{(n-N)}) \times e^{\frac{-j2\pi nk}{N}} \tag{11}$$

According to the previous there are only two multiplication processes required when calculating a new value, which will cause a time reduction during the calculation of the DFT, which means minimum lag during synchronization.

IV. The Proposed Measurement Method

There are three elements that should be found during vector measuring, which are the frequency, the magnitude and the phase angle. Ideally, grid waveform oscillate at or close to 50 Hz,where the proposed algorithm in this paper will suggest a method to found the actual value.

Because grid frequency can varied within a certain limits ,usually between 48Hz and 52Hz, the suggested algorithm will apply two DFT with different window width tuned at the same mentioned frequencies.

The chosen number of samples should be a positive integer that is multiple of both frequencies to comply with the following.

$$f_{(measured)} = \frac{k \cdot f_s}{N} \tag{12}$$

where f_s is the clock frequency.

Executing the RDFT will generate real and imaginary values that will varied according to the input in $sinc$ property for each frequency bin. Both values are centred on the selected frequencies which have a magnitude of Hb and Ha".

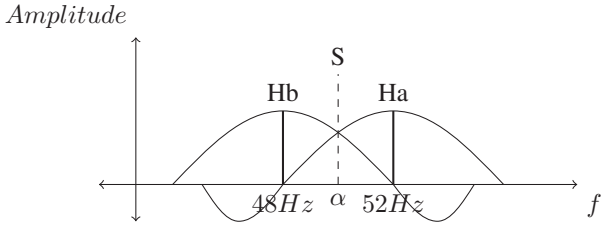

Fig. 2. shows two frequencies measurement with difference of 4Hz

As shown in Fig.2 if the grid waveform oscillate at exact 50 Hz, both of Hb and Ha will have the same value and by drawing the envelop of the $sinc$ for the two RDFT, both envelops should interact at α point.

By assuming that the grid is not oscillating at 50 Hz, the following equation can solve to find the magnitude and frequency at point α.

$$Ha \cdot sinc(52-\alpha) = S \tag{13}$$

$$Hb \cdot sinc(52-4+\alpha) = S \tag{14}$$

where Ha,Hb are unity and represent the magnitude of the measured frequency point. solving both of 13 and 14 should have the same values and can be rewritten as

$$Ha \cdot \frac{sin(52-\alpha)}{52-\alpha} = S \tag{15}$$

$$Hb \cdot \frac{sin(48+\alpha)}{48+\alpha} = S \tag{16}$$

Applying Taylor series can be one of the methods to solve the equation to find α as follows

$$sin(52-\alpha) = (52-\alpha) - \frac{(52-\alpha)^3}{3!} + \frac{(52-\alpha)^5}{5!} - \frac{(52-\alpha)^7}{7!} + \cdots \quad (17)$$

or it can be rewritten as

$$sin(52-\alpha) = \sum_{i=0}^{\infty} \frac{(-1)^i}{(2i+1)!}(52-\alpha)^{2i+1} \quad (18)$$

where i is an integer value.

As it can be seen solving the $sinc$ function can leads to a series of sequential mathematical equations which requires a huge time to be solved and leads to make the solution inefficient. To solve this obstetrical, this paper will follow linear approximation as one of the solution to reduce computational time.

Alternatively applying linear approximation to the $sinc$ functions can reduce the computational time and provide an accurate frequency measuring. It can be best described as, measuring the frequency from the amplitude. Referring to Fig.3 This can be performed by drawing a straight line between the peak of the 52 Hz point and end at 48 HZ. this will shape a triangle that has a unity hight and a width of 4 Hz.

The hight of the triangle will be changing with respect to the RDFT obtained values. This variation will lead to move the interaction point α along the scale of 4 Hz.

Practically, when $Hb = 1$ and $Ha = 0$ then the measured frequency should be 48 Hz while, if the $Hb = 0$ and $Ha = 1$ then the measured frequency should be 52 Hz. while having same value for both will indicate a 50 Hz.

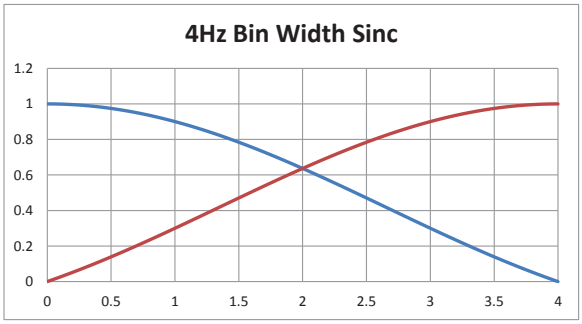

Fig. 3. two $sinc$ function interact with bin difference 4Hz

Base on the linear approximation with the aid of the regulation equation as shown below the ratio of frequency deviation can be calculated, which will lead to find the actual frequency.

$$f_{dev} = \frac{Ha}{Hb + Ha} \quad (19)$$

The previous equation will determine the value of α or the deviation in unity scale. To find the actual frequency it will be required to rescaled the deviation

$$f_{act} = 48 + 4 \times f_{dev} \quad (20)$$

Calculating the actual frequency magnitude can be a second step. It can be calculated by measuring the frequency bin amplitude in relation to the normalized amplitude. Generating a sinc lock up table based on the calculated frequency with signal magnitude of 1 amplitude and 2Hz limit can cover half the range of frequency 50-52 Hz while the second half can be mirror image. Equation (21) can be used to find the actual magnitude.

$$Amplitude = \frac{MeasuredMagnitude}{StoredMagnitude} \quad (21)$$

On the other hand, the signal phase can be calculated by using the $atan2$ function, which it uses the imaginary and the real to find the phase

Based on the proposed method there are 20 synchronization point in one cycle where:

$$Synch\ points = \frac{N_{fs}}{N} = \frac{1000}{50} = 20 \quad (22)$$

as shown in equation (15) the sampling process will repeat itself twenty times to acquire 250 sample during one duration of the grid waveform which mean high precision to resynchronize in case of frequency drifting.

V. Results and Discussion

An experimental prototype was build in order to verify the suggested method. The digital microcontroller STM32F4 discovery board by ST electronics has been programmed by the proposed algorithm. The grid voltage waveform was linked to the controller with a help of interface circuit to match the grid voltage to the controller requirement which is unipolar 3.3 Volt. System Testing was carried out to initiate the validity by checking the response speed of tracking the waveform magnitude as well as the frequency and the phase angle.

The lower waveform in Fig.4 shows a high speed of fluctuation in signal magnitude while the upper trace represents the algorithm response to the rate of change of the waveform RMS value during fluctuation.

Two advantages can be seen in Fig.4, which are the algorithm has a high response speed to the change of grid voltage and there is a linear relation in the rate of change between the measured value and the grid voltage at low frequency variation.

To ensure that the algorithm is able to synchronize an inverter with the grid accurately. Fig.5 shows a generated gate signal (pulse) of an inverter transistor that triggered at the start of each cycle of the grid waveform. It can be shown that there is a missing pulse in the waveform. This time is set to track the grid waveform in case of frequency drifting. In normal condition of operation there are another methods that can perform frequency tracking without missing a trigger.

The accuracy of measuring the frequency and the phase angle is shown in Fig. 5.The controller was able to generate a pulse at the start of each cycle of the fundamental component with no obvious delay shown. The sinusoidal waveform in Fig.5

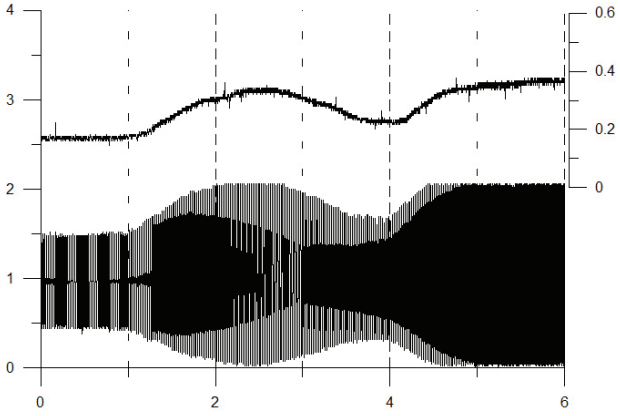

Fig. 4. speed response to input voltage variation

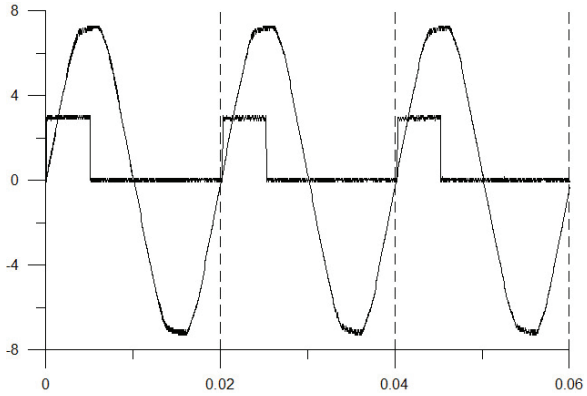

Fig. 5. Phase and Frequency Measuring accuracy

was fed from actual grid voltage which it has a continuous variation in the magnitude and the frequency.

Resynchronize for the proposed algorithm was set of 500 mSec to overcome grid frequency drifting. Fig.6 shows the Resynchronize process of the microcontroller.

The ST microcontroller was able to handle calculate the voltage waveform parameters and resynchronize by generating

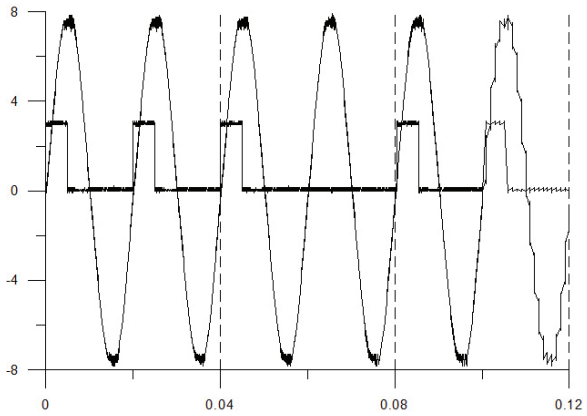

Fig. 6. Microcontroller Resynchronize

trigger pulse at each start of the fundamental cycle.

VI. Conclusion

Synchronization to a weak or distorted grid voltage with continuous frequency variation can be a problem. Usually harmonics have its effect on the sinusoidal waveform by changing it to non symmetrical signal around $\frac{\pi}{2}$. This can cause a leading or lagging in the fundamental waveform at zero-crossing point which can make many of synchronization method inefficient.

Using DFT tool with a limited window width can extract the fundamental component from the distorted signal by filtering out all high frequencies, sub-harmonics and DC component. Applying two DFT to calculate the fundamental component by implementing it using 32 bit microcontroller was successful. The controller had been able to measure, synchronise and generate trigger in real time.

The overall system efficiency can be improved by increasing the number of samples and sampling frequency, but it is subject to the faster microcontrollers. Increasing the switching frequency can help to reduce the synchronisation angle and speeds up the response to the signal magnitude changing, while increasing the number of samples can offer a better quantization in the system.

Finally, the technique was successfully passed the verification and it also offered a reduction in calculation time by using the proposed linear approximation.

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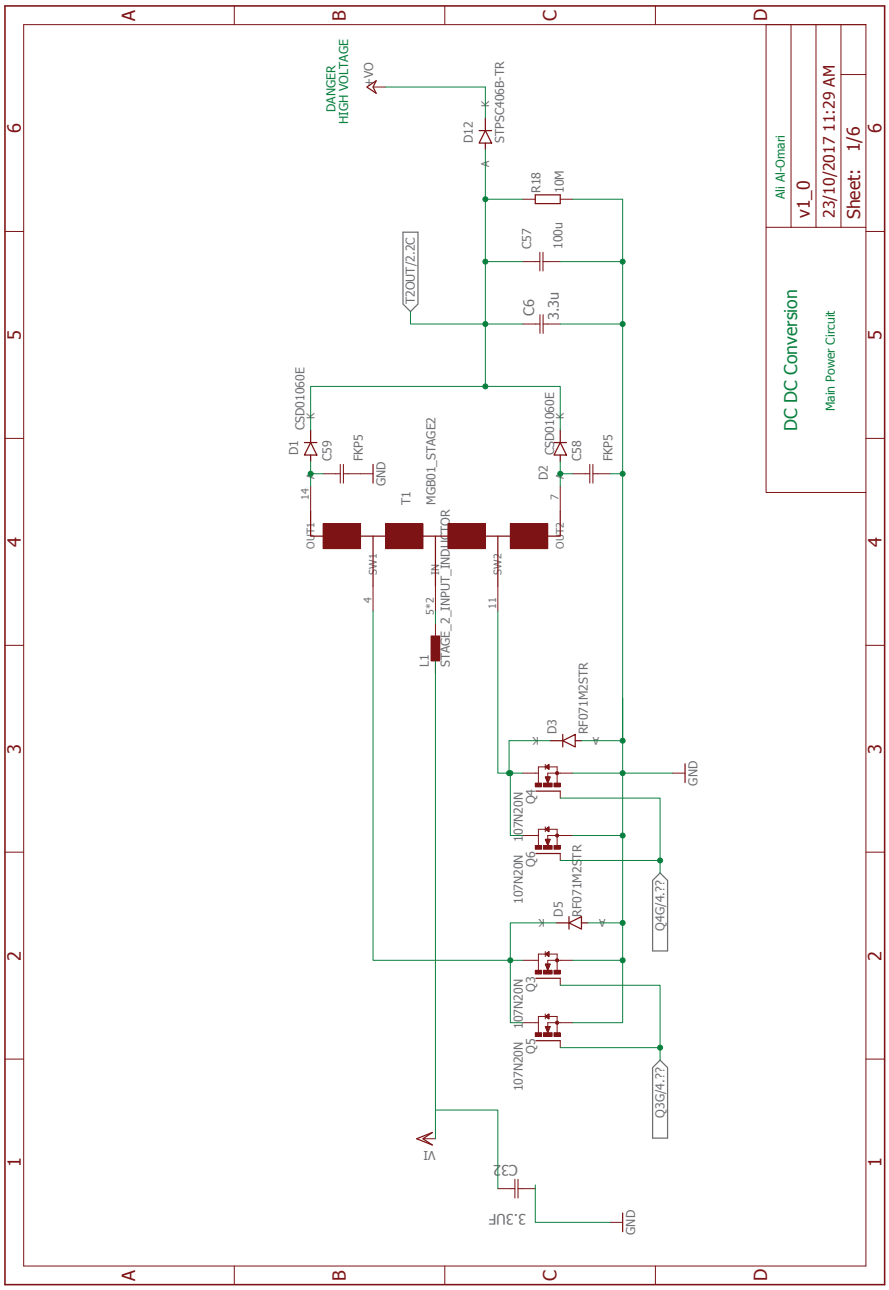
Appendix B

Circuit Diagram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VO
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STPSC406B-TR
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C57
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C6
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D1
CSD01060E
C59
FKP5
GND
T1
MGB01_STAGE2
D2
CSD01060E
C58
FKP5
L1
STAGE_2_INPUT_INDUCTOR
D3
RF071M2STR
Q4
107N20N
Q6
107N20N
D5
RF071M2STR
Q3
107N20N
Q5
107N20N
Q4G[4:??]
Q3G[4:??]
C2
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DC DC Conversion
Main Power Circuit
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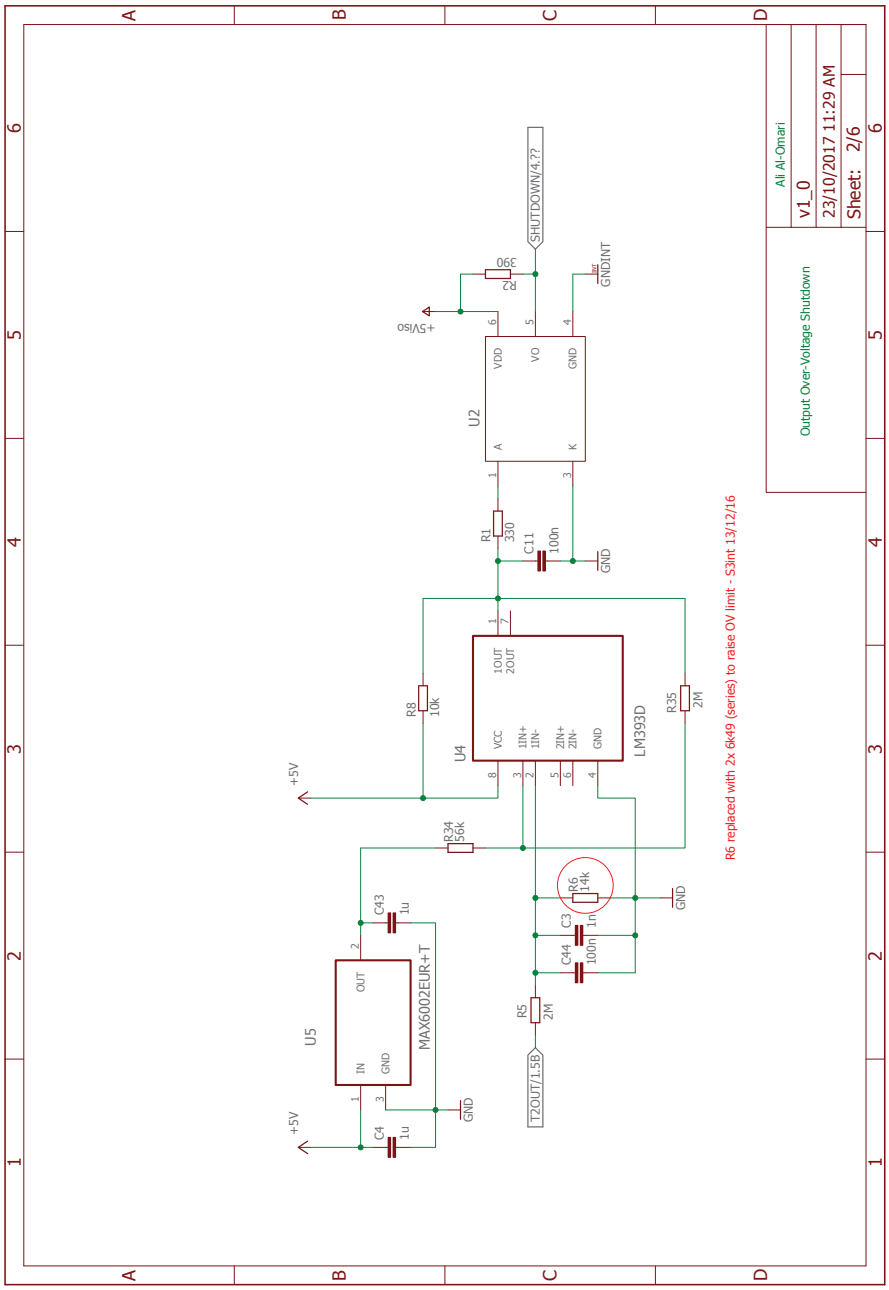
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R2
+5Viso
GNDINT
U2
VDD
VO
GND
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R1
330
C11
100n
GND
R8
10k
U4
1OUT
2OUT
VCC
1IN+
1IN-
2IN+
2IN-
GND
LM393D
R35
2M
+5V
R34
56k
R6
14k
C43
1u
C3
1n
C44
100n
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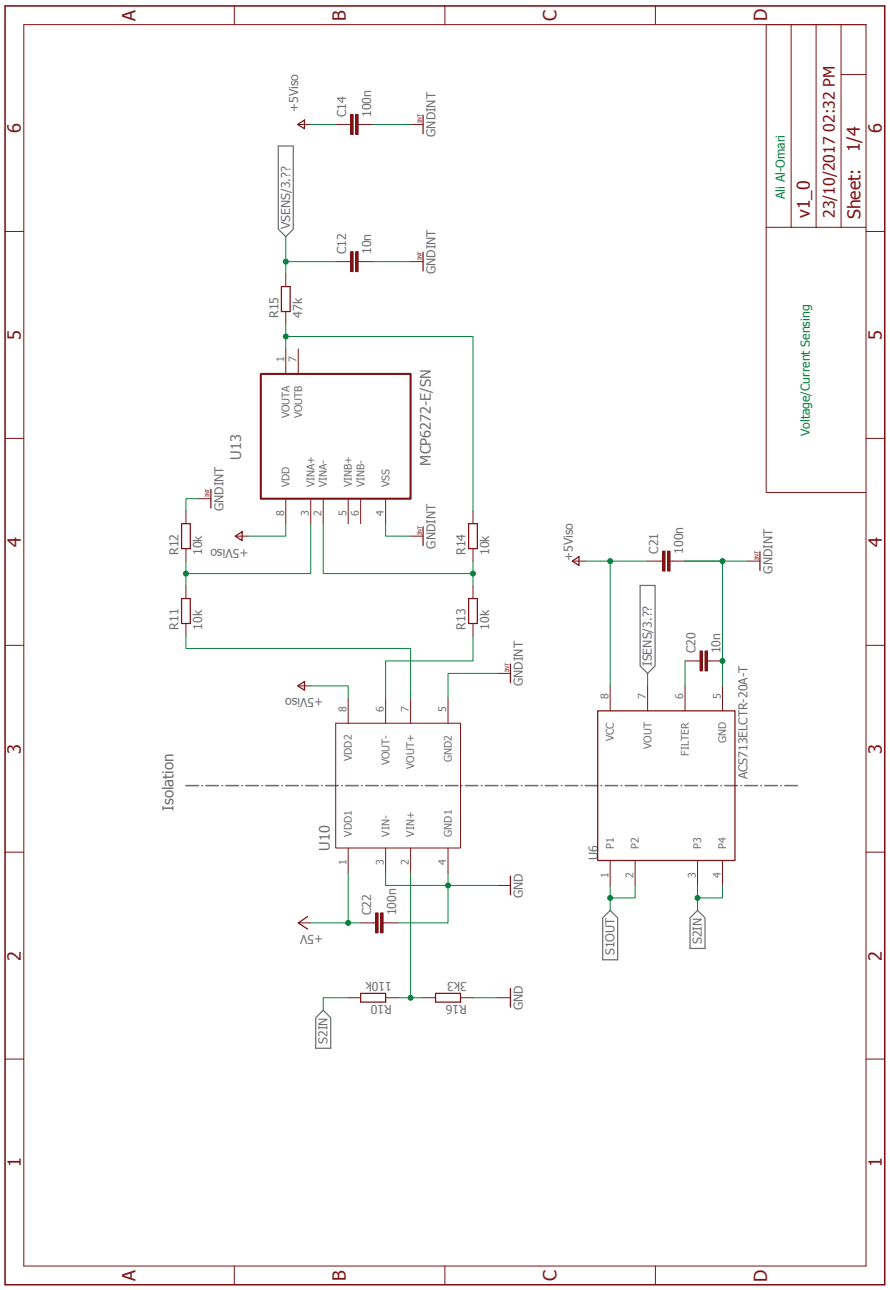
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VOUTB
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VINA+
VINA-
VINB+
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R14
10k
R11
10k
R13
10k
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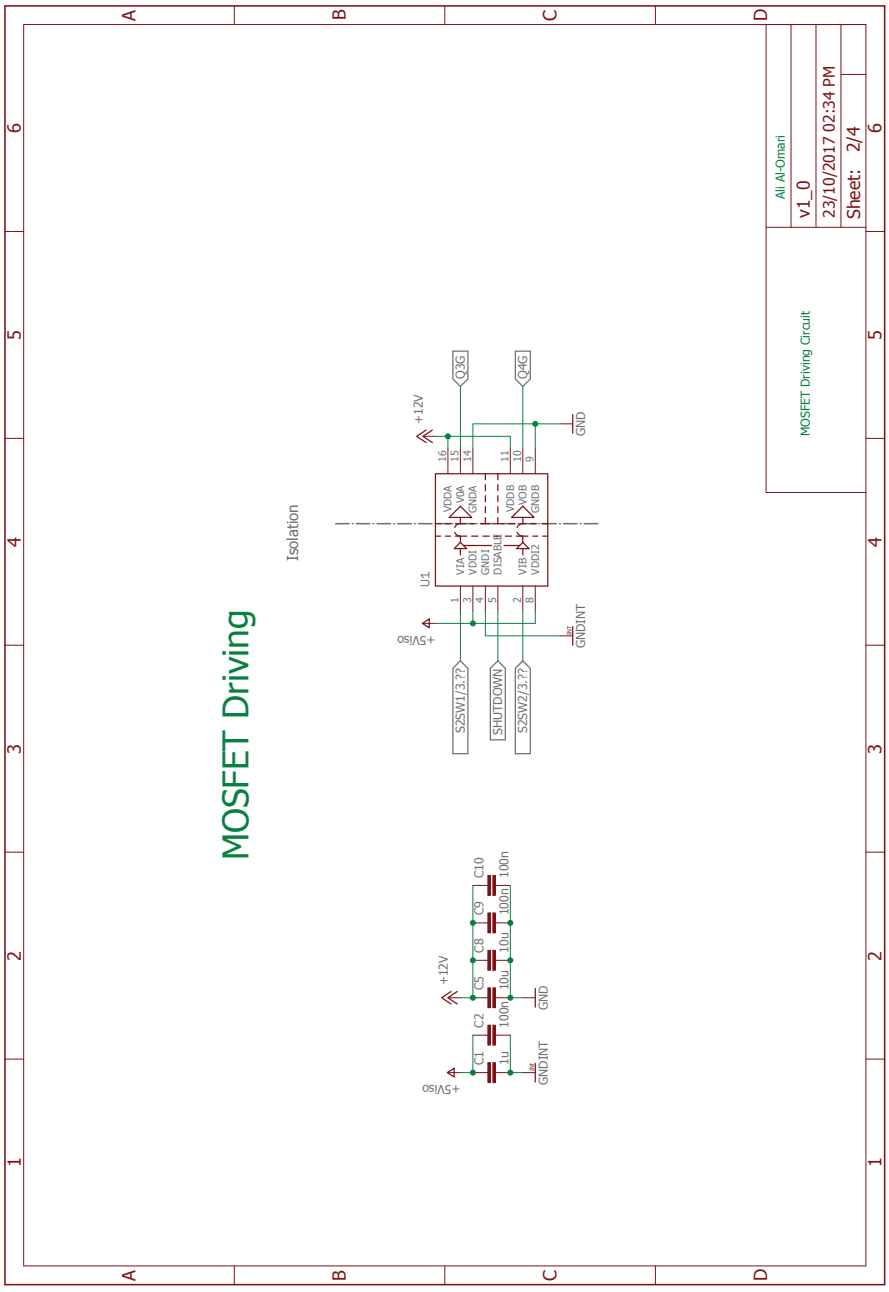
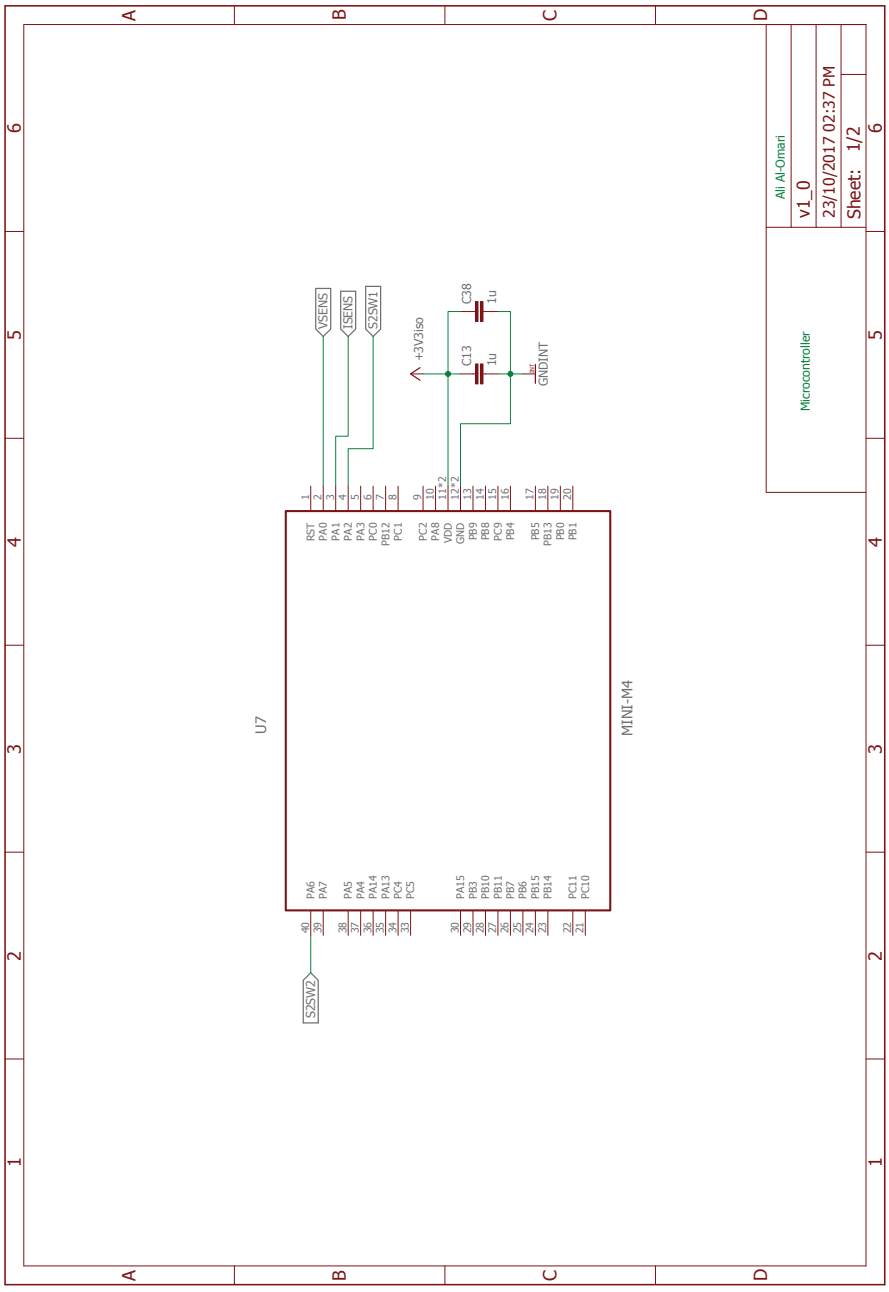
VDD2
VOUT-
VOUT+
GND2
VDD1
VIN-
VIN+
GND1
C22
100n
+5V
GND
R10
110K
R16
3K3
S2IN
C21
100n
C20
10n
ISENS/3.??
ACS713ELCTR-20A-T
VCC
VOUT
FILTER
GND
U6
P1
P2
P3
P4
S1OUT
S2IN


MOSFET Driving
Isolation
MOSFET Driving Circuit
Ali Al-Omari
v1_0
23/10/2017 02:34 PM
Sheet: 2/4
U1
+12V
GND
+5VIso
GNDINT
Q3G
Q4G
S2SW1/3.??
SHUTDOWN
S2SW2/3.??
C10
C9
C8
C5
C2
C1
100n
10u
1u


A
B
C
D
1
2
3
4
5
6
Ali Al-Omari
v1_0
23/10/2017 02:37 PM
Sheet: 1/2
Microcontroller
VSENS
TSENS
S2SW1
+3V3iso
C38
1u
C13
1u
GNDINT
U7
MINI-M4
RST
PA0
PA1
PA2
PA3
PC0
PB12
PC1
PC2
PA8
VDD
GND
PB9
PB8
PC9
PB4
PB5
PB13
PB0
PB1
PA6
PA7
PA5
PA4
PA14
PA13
PC4
PC5
PA15
PB3
PB10
PB11
PB7
PB6
PB15
PB14
PC11
PC10
S2SW2

Appendix C

Simulation Software

```
clf;

subplot(211);

fg = 51.25;
Fs = 1000;
N  = 250;
for t = 0:N-1
x(t+1) = sin(2*pi*fg*t/Fs);
plx(t+1) = t;
end

X=abs(fft(x));
stem(plx(11:16),X(11:16));
grid on
subplot(212);
grid on
xlim([40  60]);
hold on
sf = 3.9410;
fa = 48;
fb = 52;


for i= 1:100
f = (i-fg)/sf;
y(i) = X(13)*abs(mysinc(f));
ply(i) = i;
end

for i= 1:100
f = (i-fa)/sf;
y(i) = X(14)*abs(mysinc(f));
end
```

```
plot(ply(41:61),y(41:61));
for i= 1:100
f = (i-fb)/sf;
y(i) = X(13)*abs(mysinc(f));
end
plot(ply(41:61),y(41:61));
stem(fg,100);
rg = 52 - 4*(X(13)/(X(13)+X(14)));
stem(rg,100);
```

Appendix D

Synchronisation Code

```
#include "stm32f4xx.h"
#include "math.h"

// GLOBAL VARIABLES ------------------------------------------------------------

#define N 250   // Number of samples
#define k1 12   // Frequency bin for 48Hz
#define k2 13   // Frequency bin for 52Hz
#define ArrayLength 8000        // Length of array for accuracy of
                                                    frequency selection table

unsigned short int adc_data[1]; // Location to store ADC data (currently 1 sample)
float HknowRe1, HknowIm1, HkprevRe1, HkprevIm1; // Storing real and
                                                    imaginary for 48Hz
float HknowRe2, HknowIm2, HkprevRe2, HkprevIm2; // Storing real and
                                                    imaginary for 52Hz
float diff, omega;      // Storing for recursive sample difference and omega values
float omega1[250];
float omega2[250];
float cos1[250];
float sin1[250];
float phase1[250];
float phasing;
unsigned int n;         //
int current, end;       //
float Vpk1, Vpk2;       // Value for storing the
float Freq[ArrayLength];        // Array for frequency storage
float Amp[ArrayLength / 2];             // Array for amplitude storage
unsigned int point;             //
float value;    //
float frequency;        // Variable for frequency measuring
float actfreq;          // Variable for actual frequency
float amplitude;        // Variable for amplitude
float amp_norm;         // Variable for normalised amplitude
```

```
float amp_actual;       // Variable for actual  amplitude
unsigned int table_point;       // Pointer for array tables
unsigned char c;        // Used for counting in read_adc
int y1[N+1], y2[N+1];   // int ddd = 0;

float timer = 4999;
float timersync;
int timer3_val = 4999;
int npc_switch_state = 0x01;
float Phase1 , Phase2;
float PhaseOut1 , PhaseOut2 , omegaout;
unsigned int configuring =0x02;
unsigned int PhaseOutla;



// MAIN ROUTINE ------------------------------------------------------------------

int main(void)
{
//      int u;
        adc_setup(); // Setup the ADC and DAC

// CREATE TABLES FOR REDUCING COMPUTATION DURING OPERATION ----------------------

        for(point=0; point<(ArrayLength); point++)              // Create array of
                                    frequencies to reduce computation
        {
                value = (float)point;
                frequency = 48.0f + ((value / ArrayLength) * 4);
                Freq[point]  = frequency;
        }

        for(point = 0; point<(ArrayLength / 2); point++)        // Create array of
                                    magnitudes to reduce computation
                                    during run time (half size due to duplication
        {
                value = (float)point;
                if (point == 0) amplitude = 1;
                else amplitude = (sin((1.0f/4.0f)*3.14159f*(Freq[point] - 48.0f)))/(
                (1.0f/4.0f)*3.14159f*(Freq[point] - 48.0f));
                Amp[point] = amplitude;
        }
        // new points
        for(point=0; point<=249; point++)               // Create array of frequencies
                                                        to reduce computation
        {
                omega1[point] = 2 *3.14159 * (float) (point*k1)/(float)N;
                sin1[point] = sin(omega1 [point]);
                cos1[point] = cos(omega1[point]);
                phase1[point]  = atan2(sin1[point], cos1[point]);
        }

        for(point = 0; point<=249; point++)             // Create array of magnitudes to
                        reduce computation during run time (half size due to duplication)
        {
```

```
            omega2[point] = 2 *3.14159 * (float) (point*k2)/(float)N;

        }

        HknowRe1=HkprevRe1=HkprevRe1=HkprevIm1=0.0,current=0,n=0;
                                                // Reset values
        end=N;



// FOR 48Hz BIN ------------------------------------------------

y1[current]=adc_data[0];                    // store new data
diff = (float)(y1[current]-y1[end]);                // Calculate difference
                                            between new sample and old sample
omega=omega1[n];                                    // Calculate the bin
HknowRe1=HkprevRe1 + diff * cos(omega);                             // Calculate real
                                            component
HknowIm1=HkprevIm1 - diff * sin(omega);                     // Calculate imaginary
                                            component
HkprevRe1=HknowRe1;                         // Shift calculated value for next iteration
HkprevIm1=HknowIm1;                         // Shift calculated value for next iteration
Vpk1=(sqrt(HknowRe1*HknowRe1 + HknowIm1*HknowIm1)*0.0043296666f);
                                                    //Calculated magnitude at 48Hz bin
Phase1 = atan2(HknowIm1 , HknowRe1);
PhaseOut1 = ((Phase1*2047.5f/3.14159f)+2047.0f);
omegaout = ((cos(omega)*2047.5f/3.14159f)+ 2047.0f);
output_dac1 ((unsigned short int)omegaout);
output_dac2((unsigned short int)PhaseOut1);


// -FOR 52Hz BIN ------------------------------------------------------------------------

y2[current]=adc_data[0];                                    // store new data
diff = (float)(y2[current]-y2[end]);    // Calculate difference between
                                            new sample and old sample
omega = omega2[n];                                          // Calculate the bin
HknowRe2=HkprevRe2 + diff * cos(omega);         // Calculate real component
HknowIm2=HkprevIm2 - diff * sin(omega);         // Calculate imaginary component

HkprevRe2=HknowRe2;             // Shift calculated value for next iteration
HkprevIm2=HknowIm2;             // Shift calculated value for next iteration

Vpk2=(sqrt(HknowRe2*HknowRe2 + HknowIm2*HknowIm2)*0.0043296666f);       // Calculate
                                                    magnitude at 52Hz bin
Phase2 = atan2(HknowIm2, HknowRe2);
PhaseOut2 =((Phase2+3.142f)*500.0f);            // RECYCLE RECURSIVE DFT POINTERS

        if(--current<0) current=N;              //recycle pointers from recursive loop
        if(--end<0) end=N;
        if(++n==N)n=0;

// CALCULATE SIGNAL FREQUENCY / AMPLITUDE FROM LOOK UP TABLE ----------------------------

        table_point=(int)((Vpk2 / (Vpk1 + Vpk2)) * 8000.0f);    // Calculate the location
                            in the table to read frequency / normalised amplitude
```

```
actfreq = Freq[table_point];     // Get freq from the frequency table
actfreq = actfreq;

if(table_point>=4000)            // For amplitude, use the largest amplitude
                                                    side of the waveforms for accuracy
{
        amp_norm = Amp[8000-1-table_point];                 // Get the amplitude from
                                                            the amplitude table
        amp_actual=((Vpk2/amp_norm)-1.8092f)/0.3776f;       // Scale the amplitude to
                                                            the     stored amplitude
}
else
{
        amp_norm = Amp[table_point];     // Get the amplitude from the amplitude table


        amp_actual=((Vpk1/amp_norm)-1.8092f)/0.3776f;       // Scale the amplitude
                                                    to the stored amplitude
}
if(configuring == 0x02)
{
        if (PhaseOut1 >=4050)
        {
                configuring = 0x01;
        }
}
if (configuring ==0x01)
{
        if (PhaseOut1<=2048)
        {
                phasing = phase1[n];
        if (phasing<=0)
        {
                phasing = phasing + 3.14159f;
        }
        else
        {
                phasing = phasing - 3.14159f;
        }
        if (phasing <0)
        {
                phasing = 3.14159f+ (phasing + 3.14159f) ;
        }
        phasing =(phasing/(2*3.14159f));
        phasing = 1- phasing;

        timersync = (1.0f/actfreq*(1000000.0f)*(((52-actfreq)*0.1f)+0.35f + phasing));
        timer3_val = (int)(timersync);
        TIM3->CR1|=0X00;
        TIM3->CNT=0;
        TIM3->ARR= timer3_val;
        TIM3->CNT =0;
        TIM3->CR1|=0X01;
        configuring = 0x02;
        GPIOD->BSRRH = 0XF000;
        GPIOD->BSRRL = 0X6000;
```

```
                npc_switch_state =0x01;
                TIM3->SR&=~0X01;
        }
}
}
```

Appendix E

Synchronisation Setup

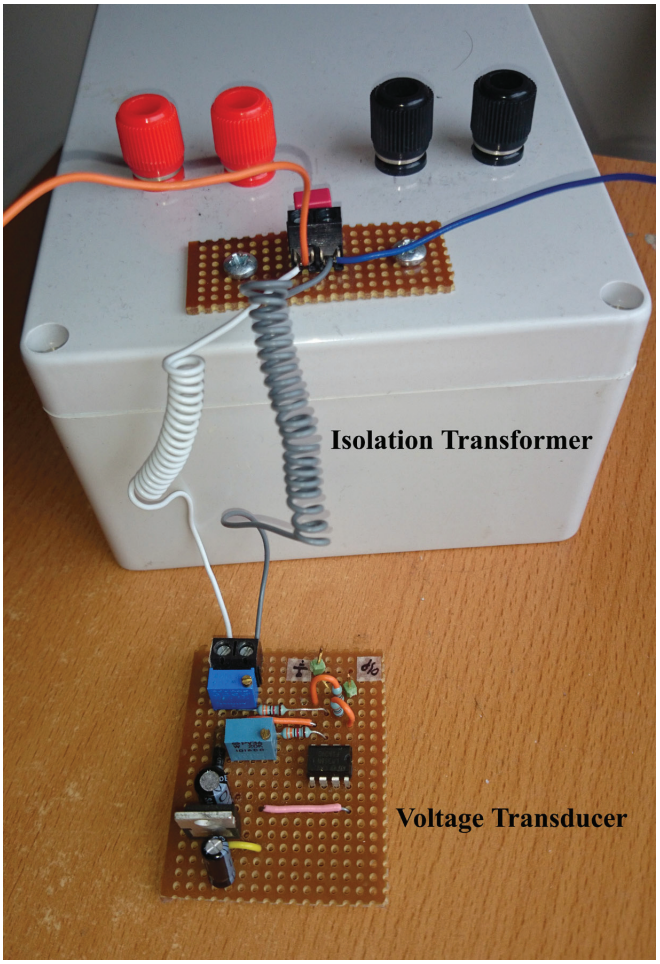


Figure E.1: Voltage Transducer and Isolation Transformer

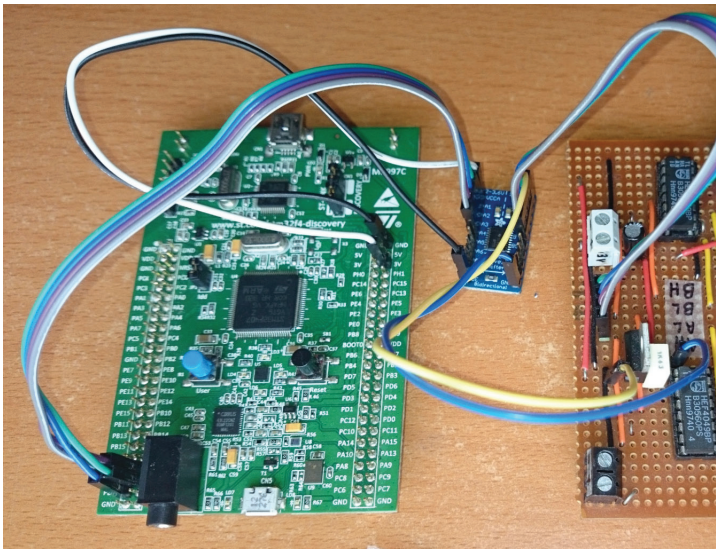


Figure E.2: Output Level Shifting Feeding Buffering Circuit

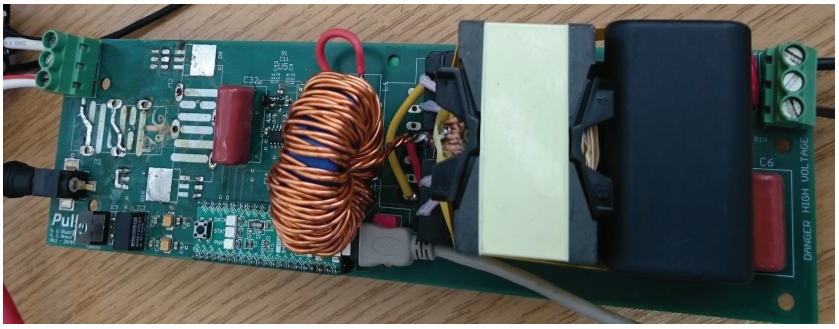


Figure E.3: DC Converter (Reversion 1) Component Side

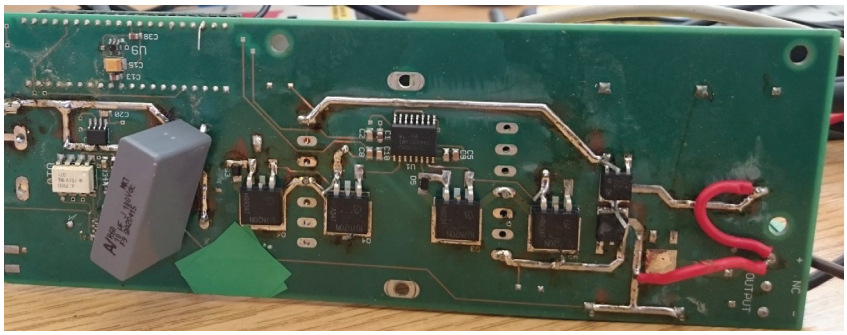


Figure E.4: DC Converter (Reversion 1) PCB Side

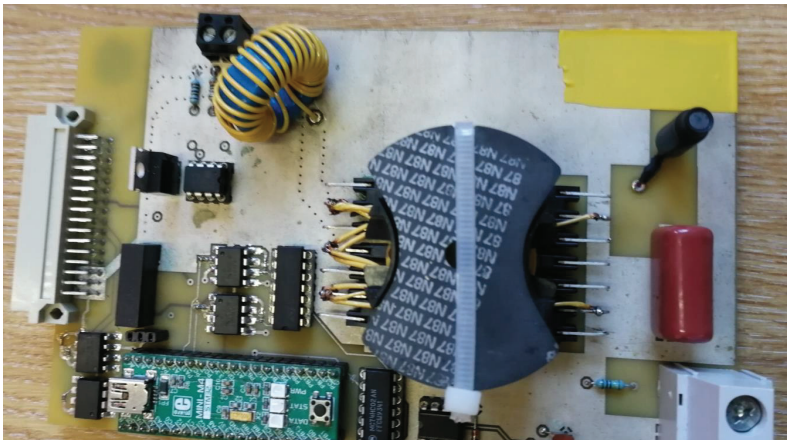


Figure E.5: DC Converter (Reversion 2) Component Side

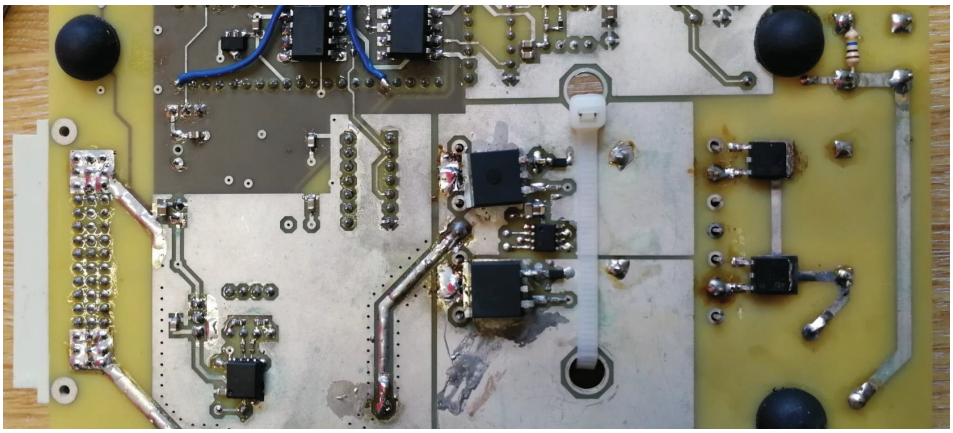


Figure E.6: DC Converter (Reversion 2) PCB Side